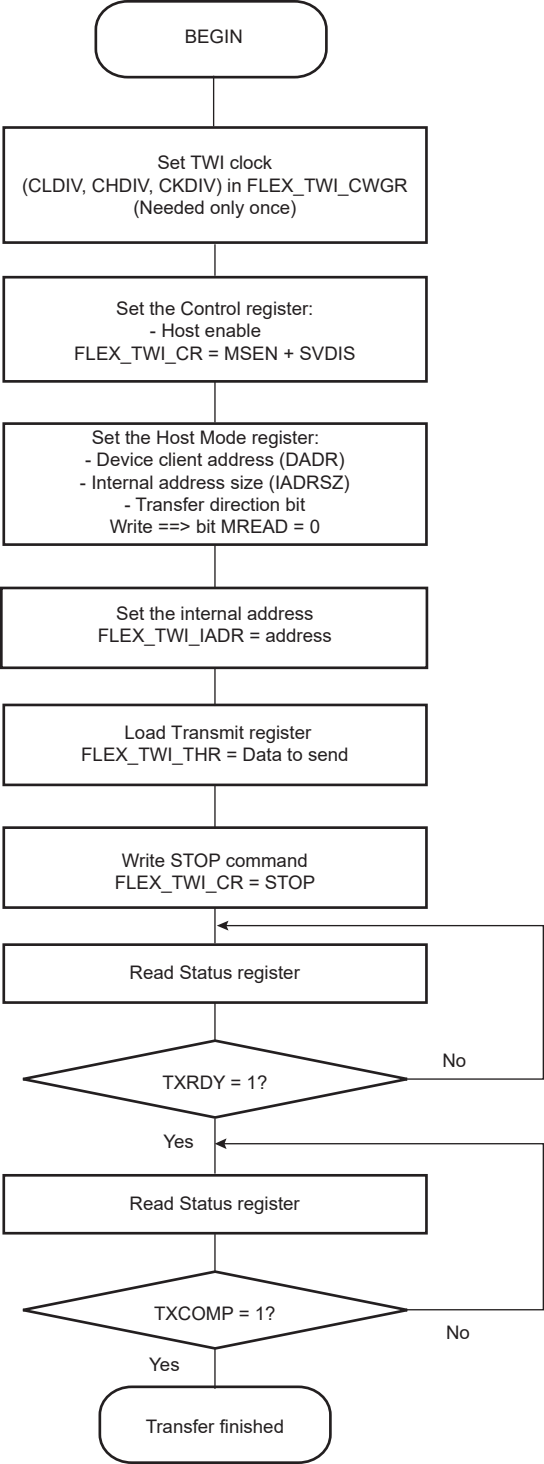
BEGIN
Set TWI clock
(CLDIV, CHDIV, CKDIV) in FLEX_TWI_CWGR
(Needed only once)
Set the Control register:
- Host enable
FLEX_TWI_CR = MSEN + SVDIS
Set the Host Mode register:
- Device client address (DADR)
- Internal address size (IADRSZ)
- Transfer direction bit
Write ==> bit MREAD = 0
Set the internal address
FLEX_TWI_IADR = address
Load Transmit register
FLEX_TWI_THR = Data to send
Write STOP command
FLEX_TWI_CR = STOP
Read Status register
TXRDY = 1?
No
Yes
Read Status register
TXCOMP = 1?
No
Yes
Transfer finished