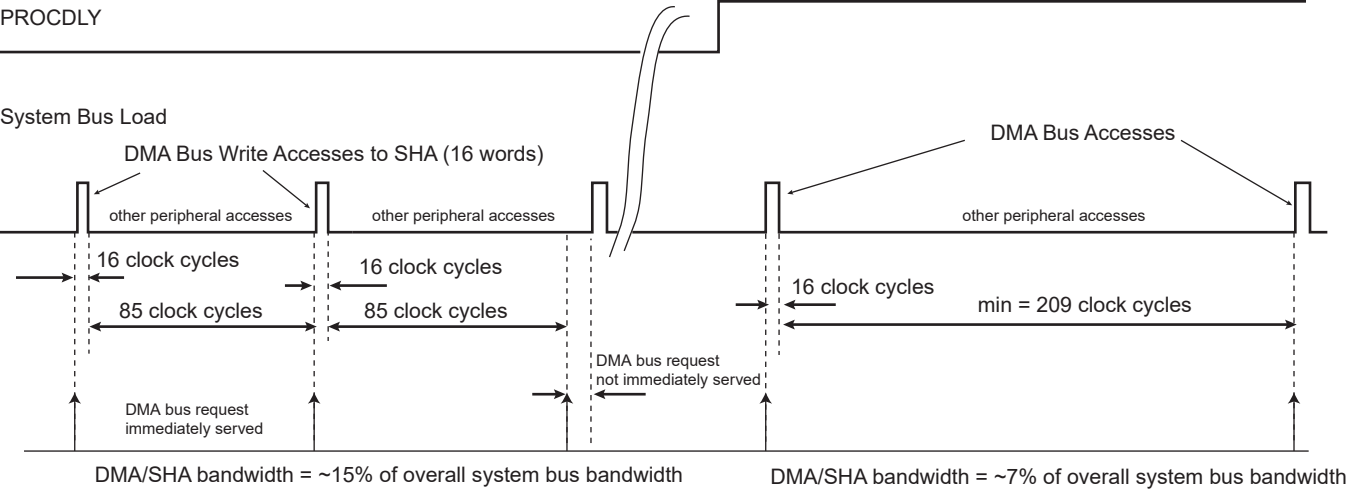
PROCDLY
System Bus Load
DMA Bus Write Accesses to SHA (16 words)
DMA Bus Accesses
other peripheral accesses
other peripheral accesses
other peripheral accesses
16 clock cycles
16 clock cycles
16 clock cycles
85 clock cycles
85 clock cycles
min = 209 clock cycles
DMA bus request
not immediately served
DMA bus request
immediately served
DMA/SHA bandwidth = ~15% of overall system bus bandwidth
DMA/SHA bandwidth = ~7% of overall system bus bandwidth