



BEGIN

Set TWIHS clock
(CLDIV, CHDIV, CKDIV) in TWIHS_CWGR
(Needed only once)

Set the Control register:
- Host enable
TWIHS_CR = MSEN + SVDIS

Set the Host Mode register:
- Device client address (DADR)
- Internal address size (IADRSZ)
- Transfer direction bit
Write ==> bit MREAD = 0

Set the internal address
TWIHS_IADR = address

Load transmit register
TWIHS_THR = Data to send

Write STOP command
TWIHS_CR = STOP

Read Status register

TXRDY = 1?

No

Yes

Read Status register

TXCOMP = 1?

No

Yes

Transfer finished