



BEGIN

Set TWIHS clock
(CLDIV, CHDIV, CKDIV) in TWIHS_CWGR
(Needed only once)

Set the Control register:
- Host enable
TWIHS_CR = MSEN + SVDIS

Set the Host Mode register:
- Device client address
- Internal address size (IADRSZ)
- Transfer direction bit
Read ==> bit MREAD = 1

Set the internal address
TWIHS_IADR = address

Start the transfer
TWIHS_CR = START | STOP

Read Status register

RXRDY = 1?

No

Yes

Read Receive Holding register

Read Status register

TXCOMP = 1?

No

Yes

END