BANK 56	BANK 57	BANK 58	BANK 59	BANK 60	BANK 61	BANK 62	BANK 63

Address	Content	Address	Content	Address	Content	Address	Content	Address	Content	Address	Content	Address	Content	Address	Content
1C00h	Core Registers	1C80h	Core Registers	1D00h	Core Registers	1D80h	Core Registers	1E00h	Core Registers	1E80h	Core Registers	1F00h	Core Registers	1F80h	Core Registers
1C0Bh		1C8Bh		1D0Bh		1D8Bh		1E0Bh		1E8Bh		1F0Bh		1F8Bh	
1C0Ch	Unimplemented Read as '0'	1C8Ch	Unimplemented Read as '0'	1D0Ch	Unimplemented Read as '0'	1D8Ch	Unimplemented Read as '0'	1E0Ch	Unimplemented Read as '0'	1E8Ch	See Table 2 for register mapping details	1F0Ch	See Table 3 for register mapping details	1F8Ch	Unimplemented Read as '0'

Bank 63 specific registers:

Address	Register
1FE3h	
1FE4h	STATUS_SHAD
1FE5h	WREG_SHAD
1FE6h	BSR_SHAD
1FE7h	PCLATH_SHAD
1FE8h	FSR0L_SHAD
1FE9h	FSR0H_SHAD
1FEAh	FSR1L_SHAD
1FEBh	FSR1H_SHAD
1FECh	—
1FEDh	STKPTR
1FEEh	TOSL
1FEFh	TOSH

Common RAM:

Bank	Range	Content
56	1C70h–1C7Fh	Common RAM (Accesses 70h-7Fh)
57	1CF0h–1CFFh	Common RAM (Accesses 70h-7Fh)
58	1D70h–1D7Fh	Common RAM (Accesses 70h-7Fh)
59	1DF0h–1DFFh	Common RAM (Accesses 70h-7Fh)
60	1E70h–1E7Fh	Common RAM (Accesses 70h-7Fh)
61	1EF0h–1EFFh	Common RAM (Accesses 70h-7Fh)
62	1F70h–1F7Fh	Common RAM (Accesses 70h-7Fh)
63	1FF0h–1FFFh	Common RAM (Accesses 70h-7Fh)

Unimplemented section end addresses: 1C6Fh, 1CEFh, 1D6Fh, 1DEFh, 1E6Fh, 1EEFh, 1F6Fh

Legend:

Unimplemented data memory locations, read as '0'