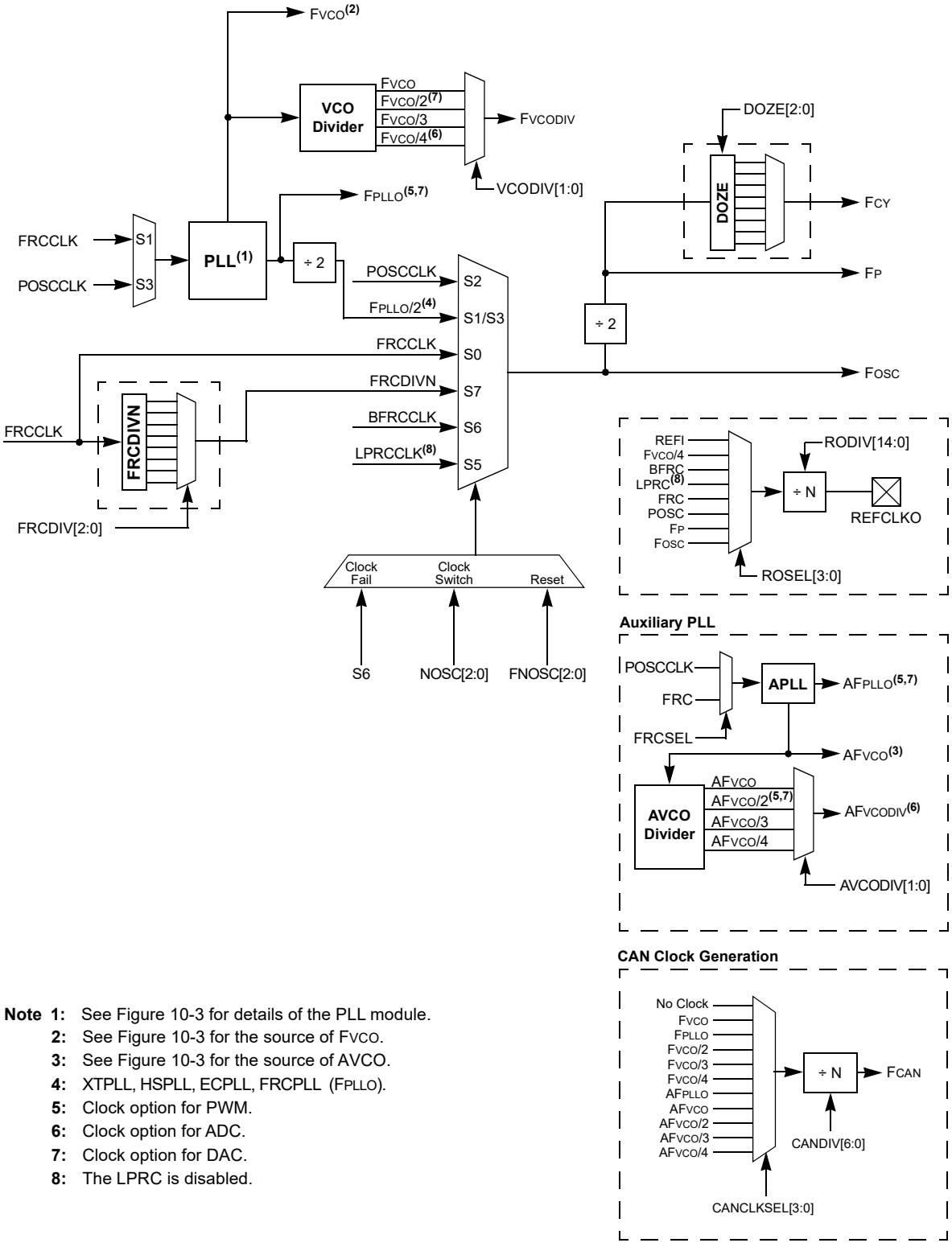

Note 1: See Figure 10-3 for details of the PLL module.
2: See Figure 10-3 for the source of FVCO.
3: See Figure 10-3 for the source of AVCO.
4: XTPLL, HSPLL, ECPLL, FRCPLL (FPLLO).
5: Clock option for PWM.
6: Clock option for ADC.
7: Clock option for DAC.
8: The LPRC is disabled.