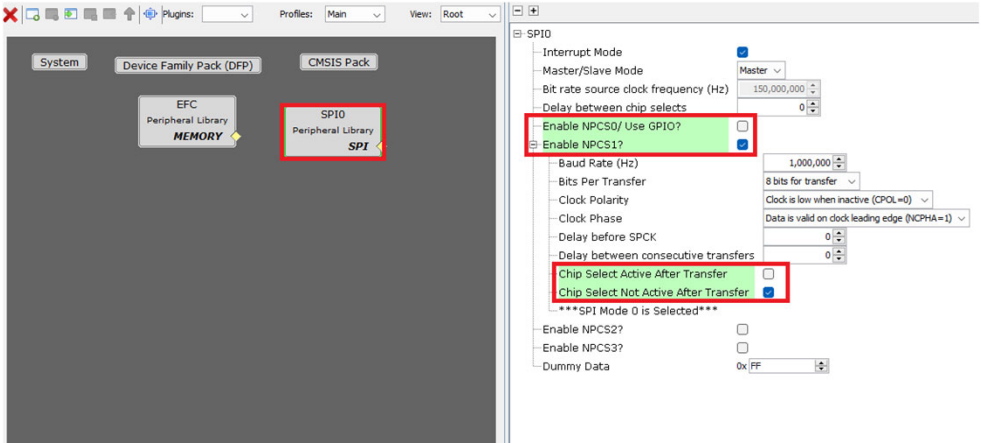
Plugins:
Profiles:
Main
View:
Root
System
Device Family Pack (DFP)
CMSIS Pack
EFC
Peripheral Library
MEMORY
SPI0
Peripheral Library
SPI
SPI0
Interrupt Mode
Master/Slave Mode
Master
Bit rate source clock frequency (Hz)
150,000,000
Delay between chip selects
0
Enable NPCS0/ Use GPIO?
Enable NPCS1?
Baud Rate (Hz)
1,000,000
Bits Per Transfer
8 bits for transfer
Clock Polarity
Clock is low when inactive (CPOL=0)
Clock Phase
Data is valid on clock leading edge (NCPHA=1)
Delay before SPCK
0
Delay between consecutive transfers
0
Chip Select Active After Transfer
Chip Select Not Active After Transfer
SPI Mode 0 is Selected
Enable NPCS2?
Enable NPCS3?
Dummy Data
0x FF