

Bit	7	6	5	4	3	2	1	0
				PDIV[3:0]				PEN
Access				R/W	R/W	R/W	R/W	R/W
Reset				1	0	0	0	1

bits 4:1 PDIV[3:0]: Prescaler Division bits

If the Prescaler Enable (PEN) bit is written to '1', these bits define the division ratio of the main clock prescaler.

Value	Description
Value	Division
0x5	64

bit 0 PEN: Prescaler Enable bit

This bit must be written '1' to enable the prescaler. When enabled, the division ratio is selected by the PDIV bit field.