| | | 1 – 1.5T$_{AD}$ | | T$_{AD}$1 | T$_{AD}$2 | T$_{AD}$3 | T$_{AD}$4 | T$_{AD}$5 | T$_{AD}$6 | T$_{AD}$7 | T$_{AD}$8 | T$_{AD}$9 | T$_{AD}$10 | T$_{AD}$11 |
| | | | | | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |

T$_{HCD}$

Conversion Starts

T$_{ACQ}$

Holding capacitor disconnected
from analog input (**T$_{HCD}$**)

On the following cycle:

ADRESH:ADRESL is loaded,
GO bit is cleared,
ADIF bit is set,
holding capacitor is reconnected to analog input.

Set GO bit

Enable ADC (ON bit)
and
select channel (CS bits)