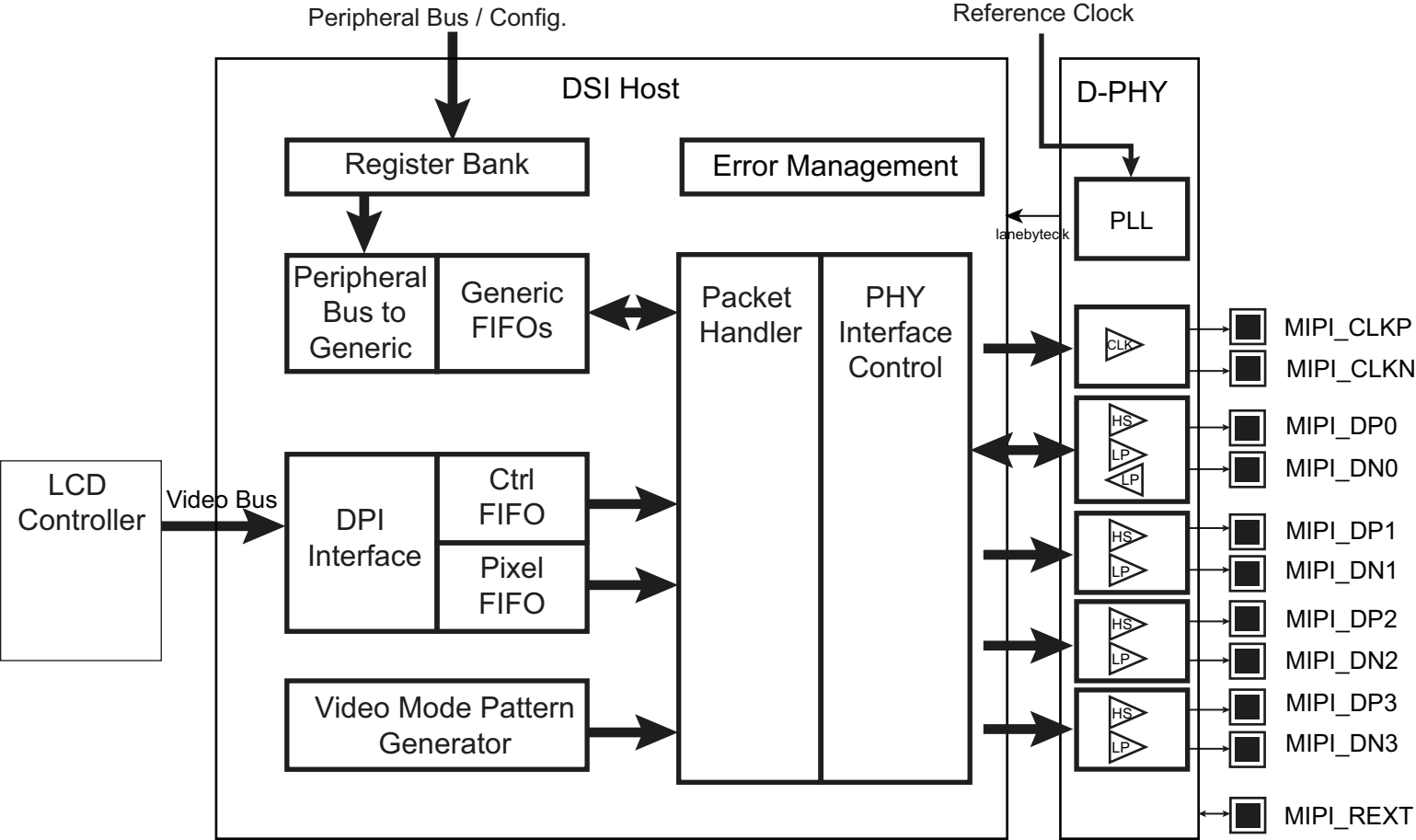
Peripheral Bus / Config.
Reference Clock
DSI Host
D-PHY
Register Bank
Error Management
PLL
lanebyteck
Peripheral Bus to Generic
Generic FIFOs
Packet Handler
PHY Interface Control
CLK
MIPI_CLKP
MIPI_CLKN
HS
LP
LP
MIPI_DP0
MIPI_DN0
LCD Controller
Video Bus
DPI Interface
Ctrl FIFO
Pixel FIFO
HS
LP
MIPI_DP1
MIPI_DN1
HS
LP
MIPI_DP2
MIPI_DN2
Video Mode Pattern Generator
HS
LP
MIPI_DP3
MIPI_DN3
MIPI_REXT