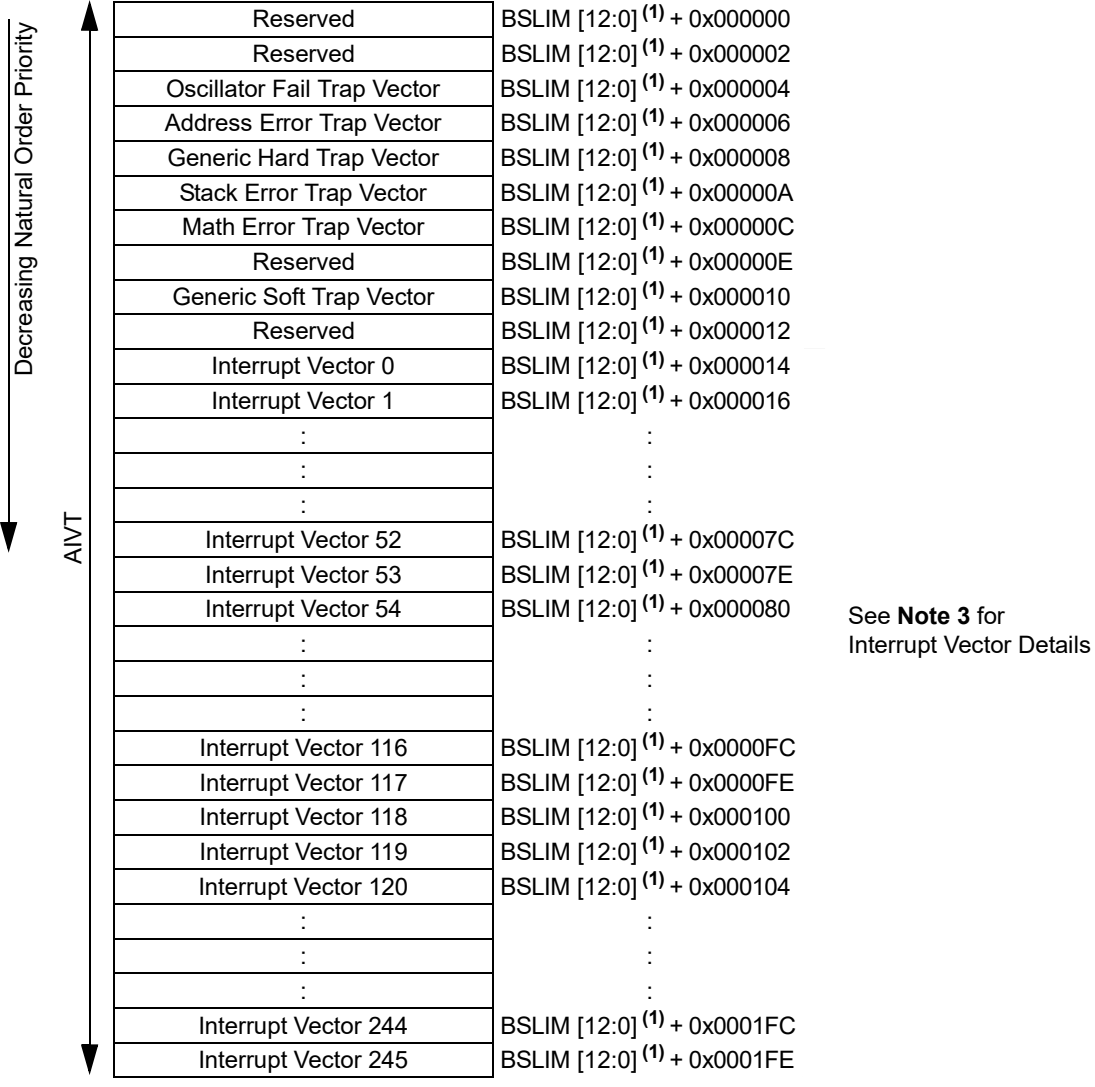
Decreasing Natural Order Priority
AIVT
Reserved
BSLIM [12:0] (1) + 0x000000
Reserved
BSLIM [12:0] (1) + 0x000002
Oscillator Fail Trap Vector
BSLIM [12:0] (1) + 0x000004
Address Error Trap Vector
BSLIM [12:0] (1) + 0x000006
Generic Hard Trap Vector
BSLIM [12:0] (1) + 0x000008
Stack Error Trap Vector
BSLIM [12:0] (1) + 0x00000A
Math Error Trap Vector
BSLIM [12:0] (1) + 0x00000C
Reserved
BSLIM [12:0] (1) + 0x00000E
Generic Soft Trap Vector
BSLIM [12:0] (1) + 0x000010
Reserved
BSLIM [12:0] (1) + 0x000012
Interrupt Vector 0
BSLIM [12:0] (1) + 0x000014
Interrupt Vector 1
BSLIM [12:0] (1) + 0x000016
Interrupt Vector 52
BSLIM [12:0] (1) + 0x00007C
Interrupt Vector 53
BSLIM [12:0] (1) + 0x00007E
Interrupt Vector 54
BSLIM [12:0] (1) + 0x000080
See Note 3 for Interrupt Vector Details
Interrupt Vector 116
BSLIM [12:0] (1) + 0x0000FC
Interrupt Vector 117
BSLIM [12:0] (1) + 0x0000FE
Interrupt Vector 118
BSLIM [12:0] (1) + 0x000100
Interrupt Vector 119
BSLIM [12:0] (1) + 0x000102
Interrupt Vector 120
BSLIM [12:0] (1) + 0x000104
Interrupt Vector 244
BSLIM [12:0] (1) + 0x0001FC
Interrupt Vector 245
BSLIM [12:0] (1) + 0x0001FE