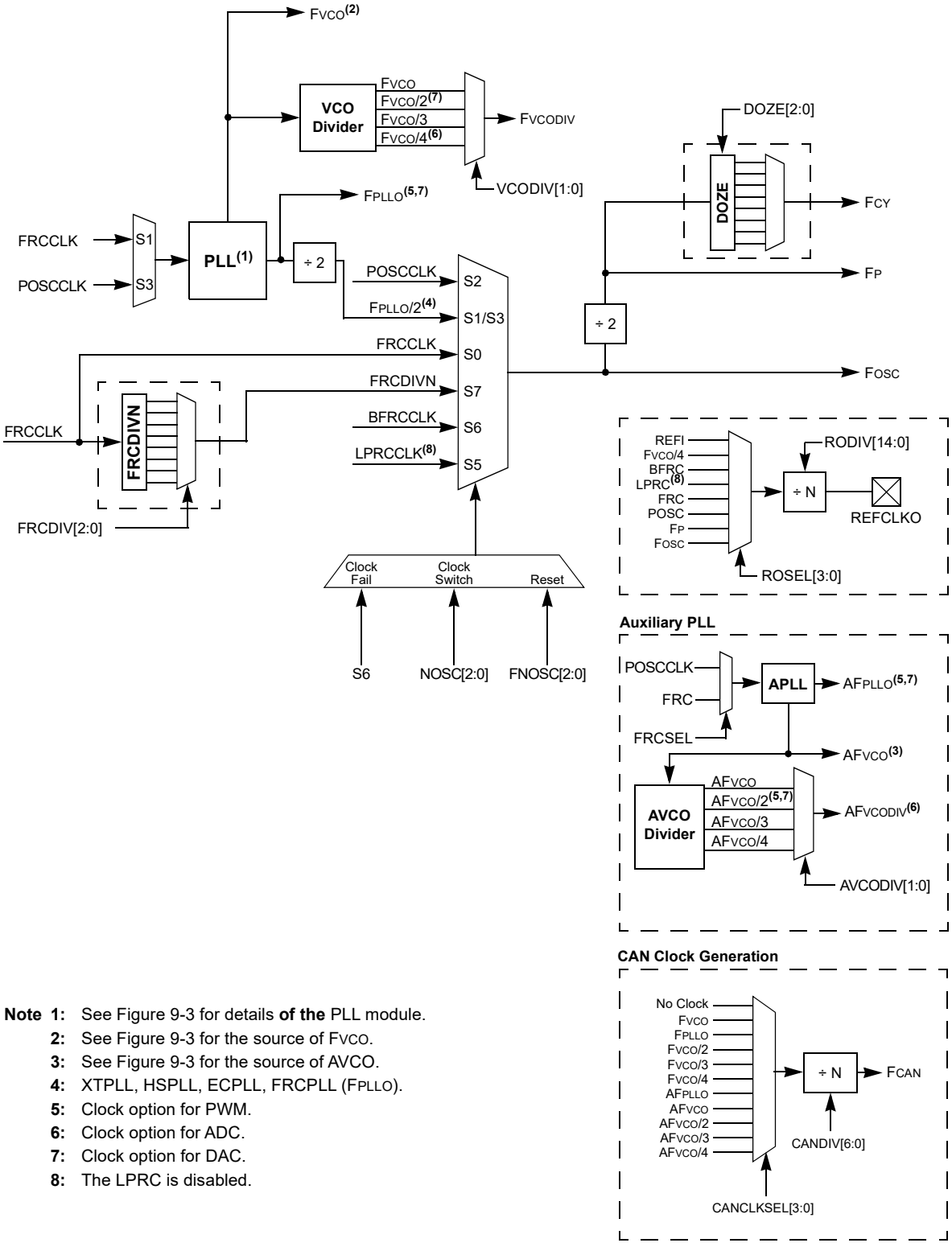

Note 1: See Figure 9-3 for details **of the** PLL module.
2: See Figure 9-3 for the source of F_{VCO}.
3: See Figure 9-3 for the source of AVCO.
4: XTPLL, HSPLL, ECPLL, FRCPLL (F_{PLLO}).
5: Clock option for PWM.
6: Clock option for ADC.
7: Clock option for DAC.
8: The LPRC is disabled.