

	BANK 56	BANK 57	BANK 58	BANK 59	BANK 60	BANK 61	BANK 62	BANK 63
1C00h	Core Registers	Core Registers	Core Registers	Core Registers	Core Registers	Core Registers	Core Registers	Core Registers
1C0Bh								
1C0Ch	Unimplemented Read as '0'	1C8Bh	1D00h	1D80h	1E00h	1E80h	1F00h	1F80h
		1C8Ch	1D0Ch	1D8Ch	1E0Bh	1E8Bh	1F0Bh	1F8Bh
		1C8Dh	1D0Dh	1D8Dh	1E0Ch	1E8Ch	1F0Ch	1F8Ch
		1C8Eh	1D0Eh	1D8Eh			1F0Dh	Unimplemented Read as '0'
		1C8Fh	1D0Fh	1D8Fh			1F0Eh	
		1C90h	1D10h	1D90h			1F0Fh	
		1C91h	1D11h	1D91h				
		1C92h	1D12h	1D92h				
		1C93h	1D13h	1D93h				
		1C94h	1D14h	1D94h				
		1C95h	1D15h	1D95h				
		1C96h	1D16h	1D96h				
		1C97h	1D17h	1D97h				
		1C98h	1D18h	1D98h				
		1C99h	1D19h	1D99h				
		1C9Ah	1D1Ah	1D9Ah				
		1C9Bh	1D1Bh	1D9Bh				
		1C9Ch	1D1Ch	1D9Ch				
		1C9Dh	1D1Dh	1D9Dh				
		1C9Eh	1D1Eh	1D9Eh				
		1C9Fh	1D1Fh	1D9Fh				
		1CA0h	1D20h	1DA0h				
		1CA1h	1D21h	1DA1h				
		1CA2h	1D22h	1DA2h				
		1CA3h	1D23h	1DA3h				
		1CA4h	1D24h	1DA4h				
		1CA5h	1D25h	1DA5h				
		Unimplemented Read as '0'	1D26h	1D26h				
			1D27h	1D27h				
			1D28h	1D28h				
			1D29h	1D29h				
			1D2Ah	1D2Ah				
	1D2Bh		1D2Bh					
	1D2Ch		1D2Ch					
	1DCDh		1DCDh					
	1D2Eh		1D2Eh					
	1D2Fh		1D2Fh					
	1D30h	1D30h						
	1D31h	1D31h						
	Unimplemented Read as '0'	1D6Fh	1D6Fh					
1C6Fh		1CEFh	1D70h	1DF0h	1E6Fh	1EEFh	1F6Fh	1FE3h
1C70h	Common RAM (Accesses 70h-7Fh)	1CF0h	1D70h	1DF0h	1E70h	1EF0h	1F70h	1FE4h
1C7Fh		1CFh	1D7Fh	1DFh	1E7Fh	1EFh	1F7Fh	1FE5h
								1FE6h
								1FE7h
								1FE8h
								1FE9h
								1FEAh
								1FEBh
								1FEC
								1FEDh
								1FEEh
								1FEFh
								1FF0h
								1FFh

Note: 1. Available on 20-pin devices only.

Legend:

Unimplemented data memory locations, read as '0'.