BANK 61

1E80h – 1E8Bh	Core Registers
1E8Ch	ANSELA
1E8Dh	WPUA
1E8Eh	ODCONA
1E8Fh	SLRCONA
1E90h	INLVLA
1E91h	IOCAP
1E92h	IOCAN
1E93h	IOCAF
1E94h	—
1E95h	—
1E96h	ANSELB(1)
1E97h	WPUB(1)
1E98h	ODCONB(1)
1E99h	SLRCONB(1)
1E9Ah	INLVLB(1)
1E9Bh	IOCBP(1)
1E9Ch	IOCBN(1)
1E9Dh	IOCBF(1)
1E9Eh	—
1E9Fh	—

1EA0h	ANSELC
1EA1h	WPUC
1EA2h	ODCONC
1EA3h	SLRCONC
1EA4h	INLVLC
1EA5h	IOCCP
1EA6h	IOCCN
1EA7h	IOCCF
1EA8h – 1EE4h	Unimplemented Read as '0'
1EE5h	RB4I2C(2)
1EE6h	RB5I2C(2)
1EE7h	RB6I2C(2)
1EE8h	RB7I2C(2)
1EE9h	RC0I2C(3)
1EEAh	RC1I2C(3)
1EEBh	—
1EECh	RC4I2C(3)
1EEDh	RC5I2C(3)
1EEEh	—
1EEFh	—
1EF0h – 1EFFh	Common RAM (Accesses 70h-7Fh)

Notes:
1. Available on 20-pin devices only.
2. Available on PIC16F17146 only.
3. Available on PIC16F17126 only.

Legend:

Unimplemented data memory locations, read as '0'.