BANK 61

1E80h	Core Registers	1EA0h	ANSELC	1EBAh	IOCEN
		1EA1h	WPUC	1EBBh	IOCEF
1E8Bh		1EA2h	ODCONC	1EBCh	Unimplemented Read as '0'
1E8Ch	ANSELA	1EA3h	SLRCONC		
1E8Dh	WPUA	1EA4h	INLVLC	1ECCh	
1E8Eh	ODCONA	1EA5h	IOCCP	1ECDh	IOCWP
1E8Fh	SLRCONA	1EA6h	IOCCN	1ECEh	IOCWN
1E90h	INLVLA	1EA7h	IOCCF	1ECFh	IOCWF
1E91h	IOCAP	1EA8h	—	1ED0h	Unimplemented Read as '0'
1E92h	IOCAN	1EA9h	—		
1E93h	IOCAF	1EAAh	ANSELD(1)	1EE2h	
1E94h	—	1EABh	WPUD(1)	1EE3h	RB1I2C
1E95h	—	1EACh	ODCOND(1)	1EE4h	RB2I2C
1E96h	ANSELB	1EADh	SLRCOND(1)	1EE5h	Unimplemented Read as '0'
1E97h	WPUB	1EAEh	INLVLD(1)		
1E98h	ODCONB	1EAFh	Unimplemented Read as '0'	1EEAh	
1E99h	SLRCONB			1EEBh	RC3I2C
1E9Ah	INLVLB	1EB3h		1EECh	RC4I2C
1E9Bh	IOCBP	1EB4h	ANSELE(1)	1EEDh	—
1E9Ch	IOCBN	1EB5h	WPUE	1EEEh	RD0I2C(1)
1E9Dh	IOCBF	1EB6h	ODCONE(1)	1EEFh	RD1I2C(1)
1E9Eh	—	1EB7h	SLRCONE(1)	1EF0h	Common RAM (Accesses 70h-7Fh)
1E9Fh	—	1EB8h	INLVLE		
		1EB9h	IOCEP	1EFFh	

Note: 1. Available on 40-pin devices only

Legend:

Unimplemented data memory locations, read as '0'