

	BANK 56		BANK 57		BANK 58		BANK 59		BANK 60		BANK 61		BANK 62		BANK 63
1C00h	Core Registers	1C80h	Core Registers	1D00h	Core Registers	1D80h	Core Registers	1E00h	Core Registers	1E80h	Core Registers	1F00h	Core Registers	1F80h	Core Registers
1C0Bh		1C88h		1D0Bh		1D8Bh		1E0Bh		1E8Bh		1F0Bh		1F8Bh	
1C0Ch	Unimplemented Read as '0'	1C8Ch	NVMADRL	1D0Ch	ADLTHL	1D8Ch	RA0PPS	1E0Ch	See Figure 9-11 for register mapping details	1E8Ch	See Figure 9-12 for register mapping details	1F0Ch	See Figure 9-13 for register mapping details	1F8Ch	Unimplemented Read as '0'
		1C8Dh	NVMADRH	1D0Dh	ADLTHH	1D8Dh	RA1PPS								
		1C8Eh	NVMDATL	1D0Eh	ADUTHL	1D8Eh	RA2PPS								
		1C8Fh	NVMDATH	1D0Fh	ADUTHH	1D8Fh	RA3PPS								
		1C90h	NVMCON1	1D10h	ADERRL	1D90h	RA4PPS								
		1C91h	NVMCON2	1D11h	ADERRH	1D91h	RA5PPS								
		1C92h	SCANLADRL	1D12h	ADSTPTL	1D92h	RA6PPS								
		1C93h	SCANLADRH	1D13h	ADSTPTH	1D93h	RA7PPS								
		1C94h	—	1D14h	ADFLTRL	1D94h	RB0PPS								
		1C95h	SCANHADRL	1D15h	ADFLTRH	1D95h	RB1PPS								
		1C96h	SCANHADRH	1D16h	ADACCL	1D96h	RB2PPS								
		1C97h	—	1D17h	ADACCH	1D97h	RB3PPS								
		1C98h	SCANCON0	1D18h	ADACCU	1D98h	RB4PPS								
		1C99h	SCANTRIG	1D19h	ADCNT	1D99h	RB5PPS								
		1C9Ah	CRCDATAI	1D1Ah	ADRPT	1D9Ah	RB6PPS								
		1C9Bh	CRCDATAH	1D1Bh	ADPREVL	1D9Bh	RB7PPS								
		1C9Ch	CRCDATAU	1D1Ch	ADPREVH	1D9Ch	RC0PPS								
		1C9Dh	CRCDATAT	1D1Dh	ADRESL	1D9Dh	RC1PPS								
		1C9Eh	CRCOUTL	1D1Eh	ADRESH	1D9Eh	RC2PPS								
		1C9Fh	CRCOUTH	1D1Fh	ADPCH	1D9Fh	RC3PPS								
		1CA0h	CRCOUTU	1D20h	ADNCH	1DA0h	RC4PPS								
		1CA1h	CRCOUTT	1D21h	ADACQL	1DA1h	RC5PPS								
		1CA2h	CRCCON0	1D22h	ADACQH	1DA2h	RC6PPS								
		1CA3h	CRCCON1	1D23h	ADCAP	1DA3h	RC7PPS								
		1CA4h	CRCCON2	1D24h	ADPREL	1DA4h	RD0PPS ⁽¹⁾								
		1CA5h	Unimplemented Read as '0'	1D25h	ADPREH	1DA5h	RD1PPS ⁽¹⁾								
				1D26h	ADCON0	1DA6h	RD2PPS ⁽¹⁾								
				1D27h	ADCON1	1DA7h	RD3PPS ⁽¹⁾							1FE3h	
				1D28h	ADCON2	1DA8h	RD4PPS ⁽¹⁾							1FE4h	STATUS_SHAD
				1D29h	ADCON3	1DA9h	RD5PPS ⁽¹⁾							1FE5h	WREG_SHAD
				1D2Ah	ADSTAT	1DAAh	RD6PPS ⁽¹⁾							1FE6h	BSR_SHAD
				1D2Bh	ADREF	1DABh	RD7PPS ⁽¹⁾							1FE7h	PCLATH_SHAD
				1D2Ch	ADACT	1DACH	RE0PPS ⁽¹⁾							1FE8h	FSROL_SHAD
				1DCDh	ADCLK	1DADh	RE1PPS ⁽¹⁾							1FE9h	FSR0H_SHAD
				1D2Eh	ADCG1A	1DAEh	RE2PPS ⁽¹⁾							1FEAh	FSR1L_SHAD
				1D2Fh	ADCG1B	1DAFh	Unimplemented Read as '0'							1FEBh	FSR1H_SHAD
				1D30h	ADCG1C									1FECh	—
				1D31h	ADCG1D ⁽¹⁾									1FEDh	STKPTR
				1D32h	ADCG1E ⁽¹⁾									1FEEh	TOSL
				1D33h - 1D6Fh	Unimplemented Read as '0'	1DEFh	Common RAM (Accesses 70h-7Fh)			1E6Fh	Common RAM (Accesses 70h-7Fh)	1EEFh	Common RAM (Accesses 70h-7Fh)	1F6Fh	Common RAM (Accesses 70h-7Fh)
1C6Fh	Common RAM (Accesses 70h-7Fh)	1CF0h	Common RAM (Accesses 70h-7Fh)	1D70h	Common RAM (Accesses 70h-7Fh)	1DF0h		1E70h	Common RAM (Accesses 70h-7Fh)	1EF0h		1F70h		1F70h	
1C70h														1FF0h	
1C7Fh		1CF7h		1D7Fh		1DF7h		1E7Fh		1EFFh		1F7Fh		1FFFh	

Note: 1. Available on 40-pin devices only

Legend:

Unimplemented data memory locations, read as '0'