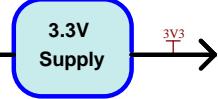
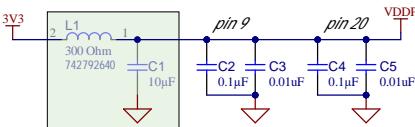


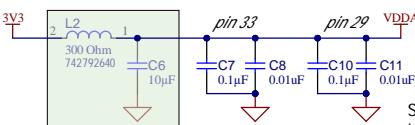
Input Power
(i.e. 12V)



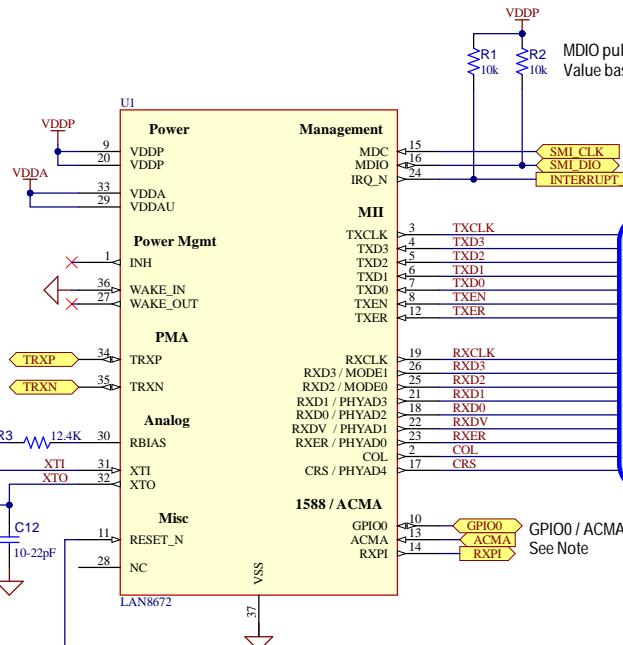
LAYOUT NOTE: Place one 0.01uF and one 0.1uF at each power pin. The 0.01uF must be closest to the pin.



Ferrite beads are optional. If used, a bulk capacitor is recommended on the device side of the ferrite bead to dampen potential oscillation.



LAN8672 MII Application - No Wake/Sleep



NOTE: If the system reset is unused, RESET_N pin can be connected directly to VDDP

from system reset

MDIO pull-up resistor:
Value based on capacitive bus loading. For light loading, 10k Ohms is a good starting value.

Serial Management Interface (SMI)

OPTIONAL: IRQ_N: If used, a pull-up resistor is required

Hardware Configuration Straps:

Values are latched upon POR RESET_N negated.

EXTERNAL RESISTORS (REQUIRED)

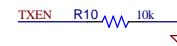
10k Ohm typical Strap resistors.
Strap resistor value is dependent on the Ethernet MAC internal resistor values.
Strap resistors must be able to override the Ethernet MAC internal pull-up or down resistor to set a logic low or high.

MODE[1:0]

00b - reserved
01b - MII with 25MHz crystal
10b - reserved
11b - reserved

PHYAD[4:0]

0x00h - 0x1fh
valid address range



NOTE: When the MAC sublayer is in reset or unconfigured, the TXEN output pin may become high impedance and floating. A pull-down can be added to prevent false TXEN assertions and accidental transmissions.

ACMA: Allows PHY to transmit to the medium.
(if unused, connect to VSS)



GPIO0: Configurable as TXPI or RXTXPI
(if unused, leave unconnected)



RXPI: Asserted when PHY receives a packet.
(if unused, leave unconnected)