| Application Active Peripheral | QTY | Peripheral Base VDDREG_IDD | Total VREG SWn CORE_IDD | Peripheral Base VDDX_IDD | Total VDDX_IDD | Total VUSB3V3 IDD | Total IOH / IOL |
|---|---|---|---|---|---|---|---|
| CPU IDD | 1 | 270 *mA* | 211 *mA*[2] | --- | --- | --- | --- |
| ADC Module | 0 | 0.6 *mA* | 0.0 *mA* | 0.5 *mA* | 0.0 *mA* | --- | --- |
| Analog Comparator | 0 | 0.5 *mA* | 0.0 *mA* | 0.3 *mA* | 0.0 *mA* | --- | --- |
| CAN_FD | 0 | 2.3 *mA* | 0.0 *mA* | --- | --- | --- | --- |
| CRYPTO (HSM) | 0 | 23 *mA* | 0 *mA* | --- | --- | --- | --- |
| DMA | 0 | 16 *mA* + 2 *mA* / Channel | 0 *mA* | 0.15 *mA* | 0.00 *mA* | --- | --- |
| EBI / SMC | 0 | 15.5 *mA* | 0.0 *mA* | 7.6 *mA* | 0.0 *mA* | --- | --- |
| Ethernet 10/100 | 0 | 11.1 *mA* | 0.0 *mA* | --- | --- | --- | --- |
| Ethernet GMII | 0 | 12.2 *mA* | 0.0 *mA* | 10.2 *mA* | 0.0 *mA* | --- | --- |
| FREQM | 0 | 1.4 *mA* | 0.0 *mA* | 0.5 *mA* | 0.0 *mA* | --- | --- |
| I2S | 0 | 2.4 *mA* | 0.0 *mA* | 0.8 *mA* | 0.0 *mA* | --- | --- |
| JTAG | 0 | 0.01 *mA* | 0.00 *mA* | --- | --- | --- | --- |
| MLB | 0 | 20 *mA* | 0 *mA* | 0.7 *mA* | 0.0 *mA* | --- | --- |
| PTC | 0 | 1.2 *mA* | 0.0 *mA* | 0.9 *mA* | 0.0 *mA* | --- | --- |
| RTC | 0 | 0.03 *mA* | 0.00 *mA* | --- | --- | --- | --- |
| SERCOM | 0 | 6 *mA* | 0 *mA* | --- | --- | --- | --- |
| SDHC | 0 | 1.4 *mA* | 0.0 *mA* | 6.3 *mA* | 0.0 *mA* | --- | --- |
| SQI | 0 | 4.6 *mA* | 0.0 *mA* | --- | --- | --- | --- |
| SWD | 0 | 0.01 *mA* | 0.00 *mA* | --- | --- | --- | --- |
| TCC | 0 | 2.1 *mA* | 0.0 *mA* | 0.5 *mA* | 0.0 *mA* | --- | --- |
| Trace | 0 | 0.01 *mA* | 0.00 *mA* | --- | --- | --- | --- |
| TRNG | 0 | 0.05 *mA* | 0.00 *mA* | --- | --- | --- | --- |
| WDT | 0 | 0.02 *mA* | 0.00 *mA* | --- | --- | --- | --- |
| | | | | | | | |
| I/O pins[1] | --- | --- | --- | --- | --- | --- | IOL = 0.0 *mA*<br>IOH = 0.0 *mA* |
| | | | | | | | |
| USB | 0 | 0 *mA* | --- | 0.5 *mA* | 0.0 *mA* | 0.0 *mA* | --- |
| PLL | 1 | 15 *mA* | --- | --- | --- | --- | --- |
| SRAM | 1 | 44 *mA* | --- | --- | --- | --- | --- |
| | | | | | | | |
| **SUB TOTAL** | --- | --- | 211.0 *mA* | --- | 0.0 *mA* | 0.0 *mA* | --- |
| **SUM TOTAL** | --- | 0.0 *mA* | | --- | 0.0 *mA* | 0.0 *mA* | --- |

NOTES:

1. This needs only to be an estimate of application total IOL sinking current & IOH sourcing current.
2. This value represents only VREG_SWn, (i.e., CORE_IDD) however the CPU IDDREG spec, (i.e., 270 mA), in the datasheet represents CPU @ 300MHz +SRAM+PLL enabled. For purposes of ensuring VREG_SWn, (i.e., CORE_IDD) load does not exceed 341 mA therefore: VALUE = (CPU IDDREG – (SRAM + PLL)) = (270mA - (44 mA+15 mA)) = 211 mA
3. VDDX = (VDDIO, AVDD, VUSB3V3) = 3.3 v, VDDREG = 1.8 v
4. Package is 208-Pin TFBGA ,($\theta_{JA}$ = 23.7 °C/W), $PD_{MAX}$ = 1.69 W
5. Rating: Industrial (-40°C ≤ Ta ≤ 85°C) Application max operating environment temperature: 85 °C

$P_{INTERNAL}$ = 0.0 ***mW*** *Requirement Satisfied (<1.69W)*

VREG_SWn CORE_IDD = 211.0 *mA* *Requirement Satisfied (<341mA)*

*Application within Safe Power Conditions*