

Application Active Peripheral	QTY	Peripheral Base VDDREG_IDD	Total VREG SWn CORE_IDD	Peripheral Base VDDX_IDD	Total VDDX_IDD	Total VUSB3V3 IDD	Total IOH / IOL
CPU IDD		<i>mA</i>	<i>mA</i> <sup>(2)</sup>	---	---	---	---
ADC Module		<i>mA</i>	<i>mA</i>	<i>mA</i>	<i>mA</i>	---	---
Analog Comparator		<i>mA</i>	<i>mA</i>	<i>mA</i>	<i>mA</i>	---	---
CAN_FD		<i>mA</i>	<i>mA</i>	---	---	---	---
CRYPTO (HSM)		<i>mA</i>	<i>mA</i>	---	---	---	---
DMA		<i>mA</i> + <i>mA</i> / Channel	<i>mA</i>	<i>mA</i>	<i>mA</i>	---	---
EBI / SMC		<i>mA</i>	<i>mA</i>	<i>mA</i>	<i>mA</i>	---	---
Ethernet 10/100		<i>mA</i>	<i>mA</i>	---	---	---	---
Ethernet GMII		<i>mA</i>	<i>mA</i>	<i>mA</i>	<i>mA</i>	---	---
FREQM		<i>mA</i>	<i>mA</i>	<i>mA</i>	<i>mA</i>	---	---
I2S		<i>mA</i>	<i>mA</i>	<i>mA</i>	<i>mA</i>	---	---
JTAG		<i>mA</i>	<i>mA</i>	---	---	---	---
MLB		<i>mA</i>	<i>mA</i>	<i>mA</i>	<i>mA</i>	---	---
PTC		<i>mA</i>	<i>mA</i>	<i>mA</i>	<i>mA</i>	---	---
RTC		<i>mA</i>	<i>mA</i>	---	---	---	---
SERCOM		<i>mA</i>	<i>mA</i>	---	---	---	---
SDHC		<i>mA</i>	<i>mA</i>	<i>mA</i>	<i>mA</i>	---	---
SQI		<i>mA</i>	<i>mA</i>	---	---	---	---
SWD		<i>mA</i>	<i>mA</i>	---	---	---	---
TCC		<i>mA</i>	<i>mA</i>	<i>mA</i>	<i>mA</i>	---	---
Trace		<i>mA</i>	<i>mA</i>	---	---	---	---
TRNG		<i>mA</i>	<i>mA</i>	---	---	---	---
WDT		<i>mA</i>	<i>mA</i>	---	---	---	---
I/O pins <sup>(1)</sup>	---	---	---	---	---	---	IOL = <i>mA</i> IOH = <i>mA</i>
USB			---	<i>mA</i>	<i>mA</i>	<i>mA</i>	---
PLL			---	---	---	---	---
SRAM			---	---	---	---	---
<b>SUB TOTAL</b>	---	---		---		<i>mA</i>	---
<b>SUM TOTAL</b>	---			---			---

NOTES:

1. This needs only to be an estimate of application total IOL sinking current & IOH sourcing current.
2. This value represents only VREG\_SWn, (i.e., CORE\_IDD) however the CPU IDDREG spec, (i.e., 270 mA), in the datasheet represents CPU @ 300MHz +SRAM+PLL enabled. For purposes of ensuring VREG\_SWn, (i.e., CORE\_IDD) load does not exceed 341 mA therefore: VALUE = (CPU IDDREG – (SRAM + PLL)) = (270mA - (44 mA+15 mA)) = 211 mA
3.  $VDDX = (VDDIO, AVDD, VUSB3V3) = \quad v$ ,  $VDDREG = \quad v$
4. Package is  $\quad$ ,  $(\theta_{JA} = \quad \text{°C/W})$ ,  $PD_{MAX} = \quad W$
5. Rating:  $\quad$  Application max operating environment temperature:  $\quad \text{°C}$

$P_{INTERNAL} = \quad mW$

$VREG\_SWn\ CORE\_IDD = \quad mA$