

**BANK 61**

1E80h	Core Registers	1EAAh	ANSELD <sup>(1)</sup>
1E8Bh		1EABh	WPUD <sup>(1)</sup>
1E8Ch	ANSELA	1EACH	ODCOND <sup>(1)</sup>
1E8Dh	WPUA	1EADh	SLRCOND <sup>(1)</sup>
1E8Eh	ODCONA	1EAEh	INLVLD <sup>(1)</sup>
1E8Fh	SLRCONA	1EAFh	Unimplemented Read as '0'
1E90h	INLVLA	1EB3h	
1E91h	IOCAP	1EB4h	ANSELE
1E92h	IOCAN	1EB5h	WPUE
1E93h	IOCAF	1EB6h	ODCONE
1E94h	—	1EB7h	SLRCONE
1E95h	—	1EB8h	INLVLE
1E96h	ANSELB	1EB9h	IOCEP
1E97h	WPUB	1EBAh	IOCEN
1E98h	ODCONB	1EBBh	IOCEF
1E99h	SLRCONB	1EBCh	Unimplemented Read as '0'
1E9Ah	INLVLB	1EE2h	
1E9Bh	IOCBP	1EE3h	RB1I2C
1E9Ch	IOCBN	1EE4h	RB2I2C
1E9Dh	IOCBF	1EE5h	Unimplemented Read as '0'
1E9Eh	—	1EEAh	
1E9Fh	—	1EEBh	RC3I2C
1EA0h	ANSELC	1EECh	RC4I2C
1EA1h	WPUC	1EEDh	—
1EA2h	ODCONC	1EEeh	RD0I2C <sup>(1)</sup>
1EA3h	SLRCONC	1EEFh	RD1I2C <sup>(1)</sup>
1EA4h	INLVLC	1EF0h	Common RAM (Accesses 70h-7Fh)
1EA5h	IOCCP	1EFFh	
1EA6h	IOCCN		
1EA7h	IOCCF		
1EA8h	—		
1EA9h	—		

**Note:** 1. Available on 40/44-pin devices only

Legend:



Unimplemented data memory locations, read as '0'