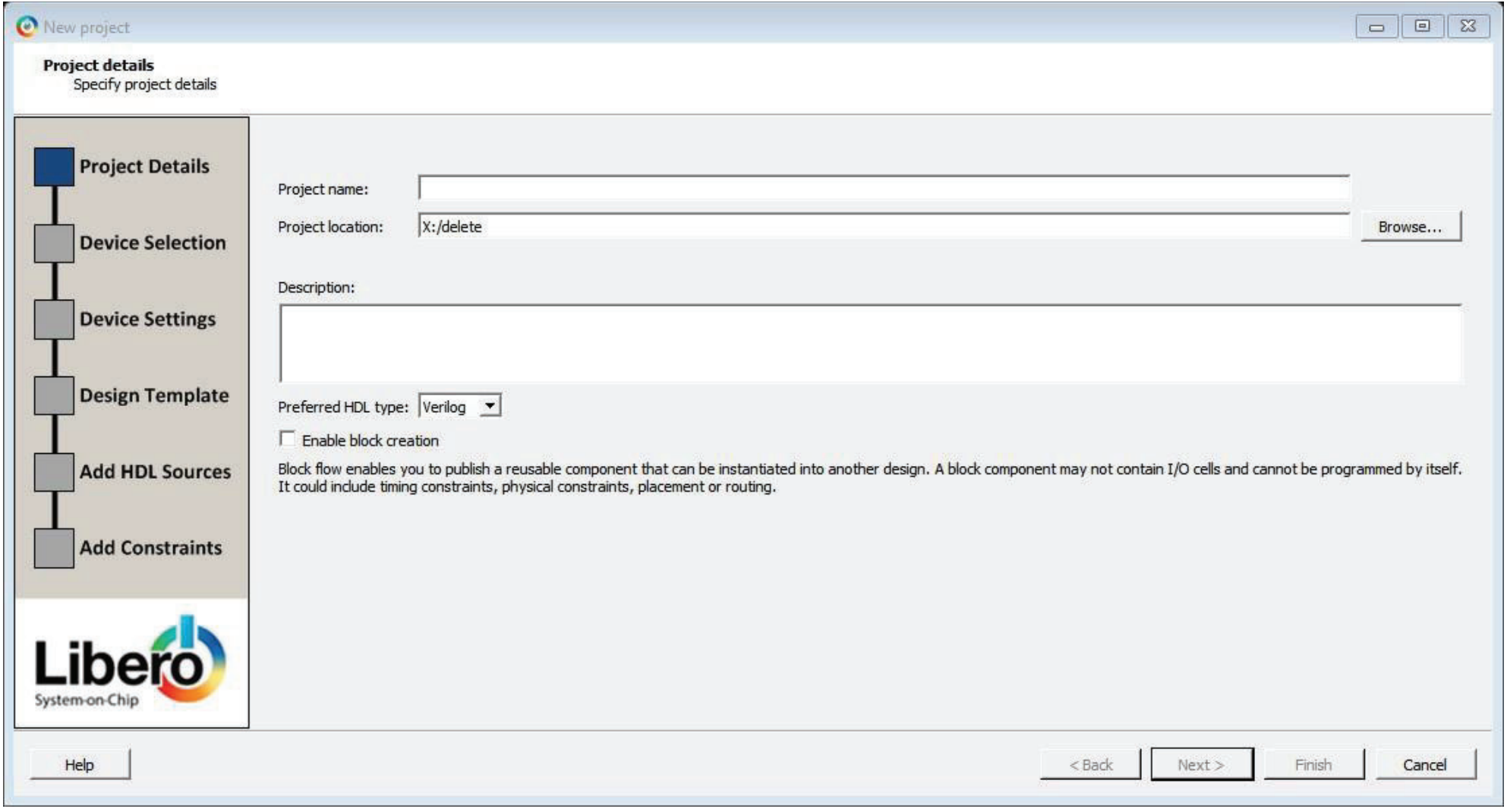
New project
Project details
Specify project details
Project Details
Device Selection
Device Settings
Design Template
Add HDL Sources
Add Constraints
Libero
System-on-Chip
Project name:
Project location:
X:/delete
Browse...
Description:
Preferred HDL type:
Verilog
Enable block creation
Block flow enables you to publish a reusable component that can be instantiated into another design. A block component may not contain I/O cells and cannot be programmed by itself. It could include timing constraints, physical constraints, placement or routing.
Help
< Back
Next >
Finish
Cancel