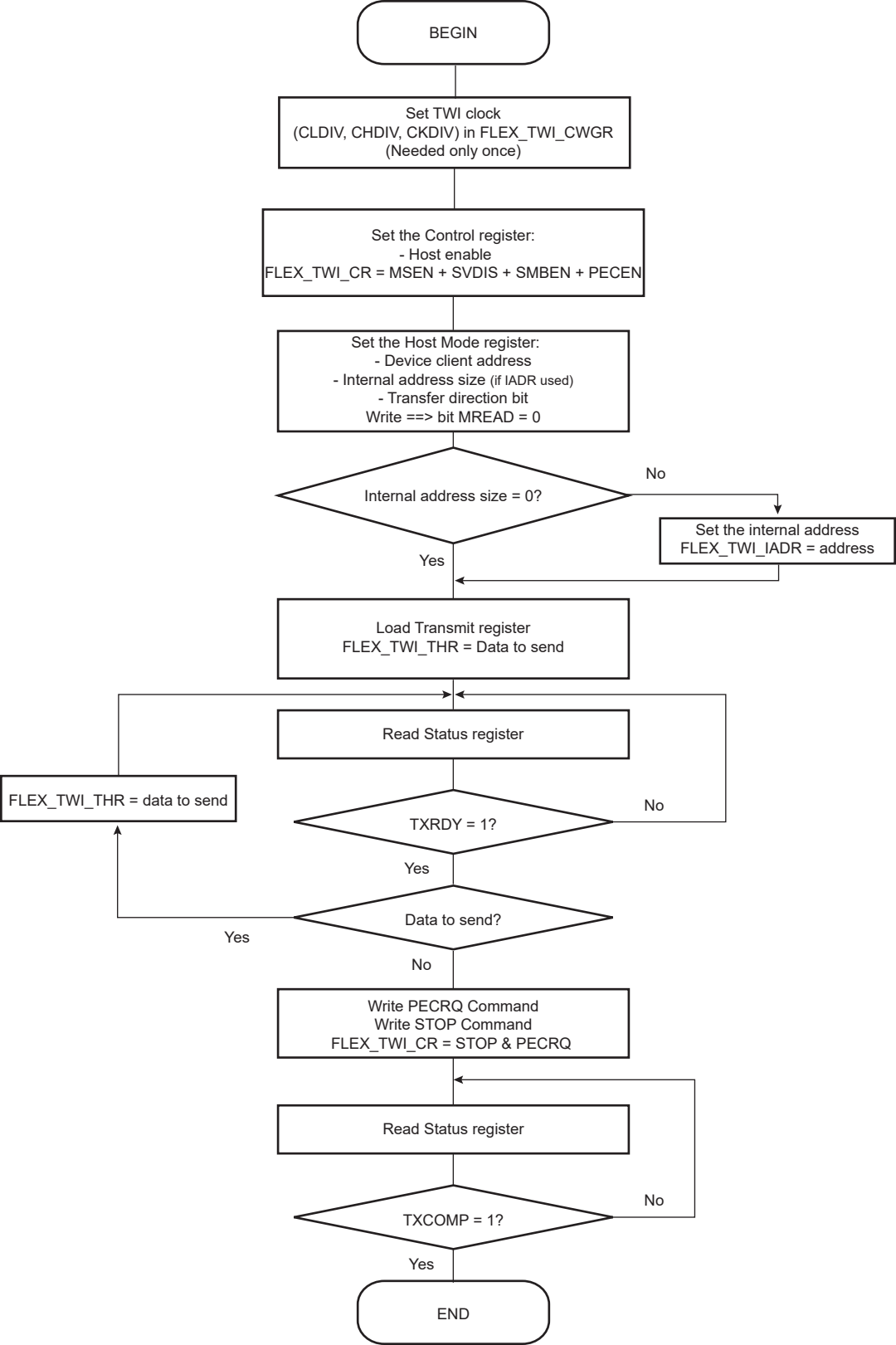
BEGIN
Set TWI clock
(CLDIV, CHDIV, CKDIV) in FLEX_TWI_CWGR
(Needed only once)
Set the Control register:
- Host enable
FLEX_TWI_CR = MSEN + SVDIS + SMBEN + PECEN
Set the Host Mode register:
- Device client address
- Internal address size (if IADR used)
- Transfer direction bit
Write ==> bit MREAD = 0
Internal address size = 0?
No
Set the internal address
FLEX_TWI_IADR = address
Yes
Load Transmit register
FLEX_TWI_THR = Data to send
Read Status register
FLEX_TWI_THR = data to send
TXRDY = 1?
No
Yes
Data to send?
Yes
No
Write PECRQ Command
Write STOP Command
FLEX_TWI_CR = STOP & PECRQ
Read Status register
TXCOMP = 1?
No
Yes
END