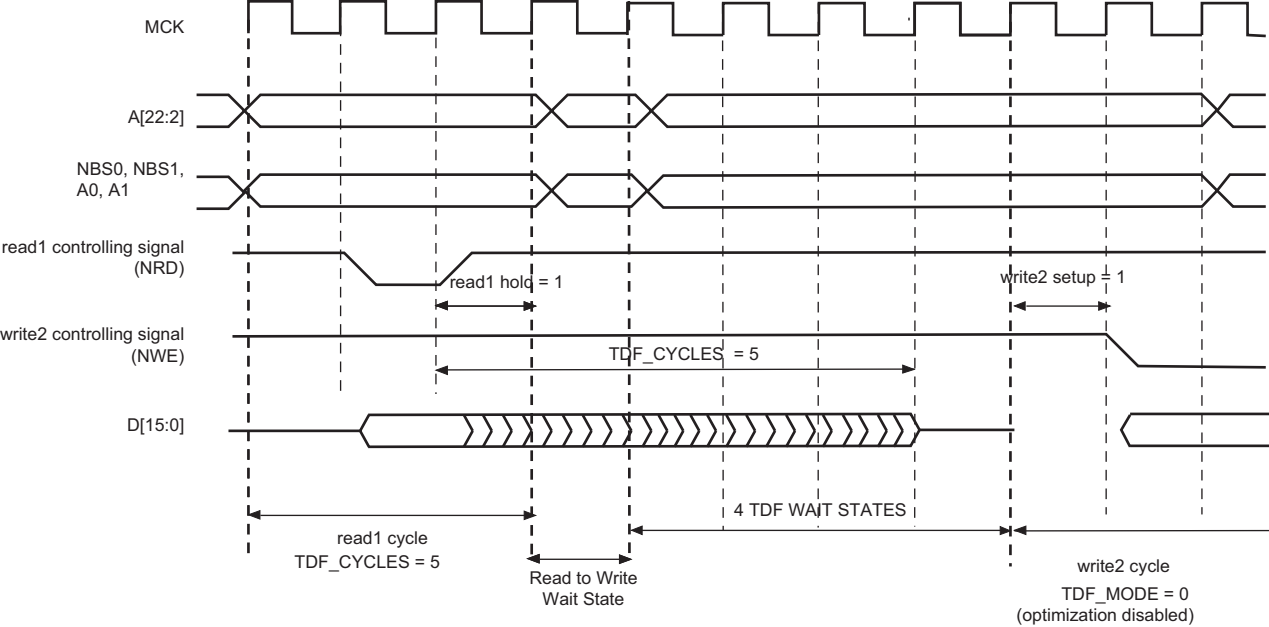
MCK
A[22:2]
NBS0, NBS1,
A0, A1
read1 controlling signal
(NRD)
read1 hold = 1
write2 setup = 1
write2 controlling signal
(NWE)
TDF_CYCLES = 5
D[15:0]
4 TDF WAIT STATES
read1 cycle
TDF_CYCLES = 5
Read to Write
Wait State
write2 cycle
TDF_MODE = 0
(optimization disabled)