

BANK 56		BANK 57		BANK 58		BANK 59		BANK 60		BANK 61		BANK 62		BANK 63				
1C00h	Core Registers	1C80h	Core Registers	1D00h	Core Registers	1D80h	Core Registers	1E00h	Core Registers	1E80h	Core Registers	1F00h	Core Registers	1F80h	Core Registers			
1C0Bh	Unimplemented Read as '0'	1C8Bh	Unimplemented Read as '0'	1D00h	ADLTHL	1D8Bh	RA0PPS	1E0Bh	See Figure 9-11 for register mapping details	1E8Bh	See Figure 9-12 for register mapping details	1F0Bh	UMTOAP	1F8Bh	Unimplemented Read as '0'			
1C0Ch		1C8Ch		NVMADL	1D00h	ADLTHH	1D8Ch	RA1PPS		1E0Ch		1E8Ch	1F0Ch	UMTOAL		1F8Ch		
		1C8Dh		NVMADH	1D00h	ADUTHL	1D8Eh	RA2PPS					1F0Eh	UMTOAH				
		1C8Eh		NVMDATL	1D00h	ADUTHH	1D8Fh	RA3PPS					1F0Fh					
		1C8Fh		NVMDATH	1D00h	ADERRL	1D90h	RA4PPS										
		1C90h		NVMCON1	1D00h	ADERRH	1D91h	RA5PPS										
		1C91h		NVMCON2	1D00h	ADSTPTL	1D92h	RA6PPS										
		1C92h		SCANLADRL	1D00h	ADSTPTH	1D93h	RA7PPS										
		1C93h		SCANLADRH	1D00h	ADFLTRL	1D94h	RB0PPS										
		1C94h		—	1D00h	ADFLTRH	1D95h	RB1PPS										
		1C95h		SCANHADRL	1D00h	ADACCL	1D96h	RB2PPS										
		1C96h		SCANHADRH	1D00h	ADACCH	1D97h	RB3PPS										
		1C97h		—	1D00h	ADACCU	1D98h	RB4PPS										
		1C98h		SCANCON	1D00h	ADCNT	1D99h	RB5PPS										
		1C99h		SCANTRIG	1D00h	ADRPT	1D9Ah	RB6PPS										
		1C9Ah		CRCDATAL	1D00h	ADPREVL	1D9Bh	RB7PPS										
		1C9Bh		CRCDATAH	1D00h	ADPREVH	1D9Ch	RC0PPS										
		1C9Ch		CRCDATAU	1D00h	ADRESL	1D9Dh	RC1PPS										
		1C9Dh		CRCDATAT	1D00h	ADRESH	1D9Eh	RC2PPS										
		1C9Eh		CRCOUTL	1D00h	ADPCH	1D9Fh	RC3PPS										
		1C9Fh		CRCOUTH	1D00h	ADNCH	1DA0h	RC4PPS										
		1CA0h		CRCOUTU	1D00h	ADACQL	1DA1h	RC5PPS										
		1CA1h		CRCOUTT	1D00h	ADACQH	1DA2h	RC6PPS										
		1CA2h		CRCCONO	1D00h	ADCAP	1DA3h	RC7PPS										
		1CA3h		CRCCON1	1D00h	ADPREL	1DA4h	RD0PPS <sup>(1)</sup>										
		1CA4h		CRCCON2	1D00h	ADPREH	1DA5h	RD1PPS <sup>(1)</sup>										
		1CA5h		Unimplemented Read as '0'	1D00h	ADCON0	1DA6h	RD2PPS <sup>(1)</sup>										
					1D00h	ADCON1	1DA7h	RD3PPS <sup>(1)</sup>										
					1D00h	ADCON2	1DA8h	RD4PPS <sup>(1)</sup>										
					1D00h	ADCON3	1DA9h	RD5PPS <sup>(1)</sup>										
					1D00h	ADSTAT	1DAAh	RD6PPS <sup>(1)</sup>										
		1D00h	ADREF		1DABh	RD7PPS <sup>(1)</sup>												
		1D00h	ADACT		1DACH	RE0PPS												
		1D00h	ADCLK		1DADh	RE1PPS												
		1D00h	ADCG1A		1DAEh	RE2PPS												
		1D00h	ADCG1B		1DAFh	Unimplemented Read as '0'												
		1D00h	ADCG1C															
		1D00h	ADCG1D <sup>(1)</sup>															
		1D00h	ADCG1E															
		1D00h	Unimplemented Read as '0'															
		1D00h																
1C6Fh	Common RAM (Accesses 70h-7Fh)	1CEFh	Common RAM (Accesses 70h-7Fh)	1D6Fh	Common RAM (Accesses 70h-7Fh)	1DEFh	Common RAM (Accesses 70h-7Fh)	1E6Fh	Common RAM (Accesses 70h-7Fh)	1EEFh	Common RAM (Accesses 70h-7Fh)	1F6Fh	Common RAM (Accesses 70h-7Fh)	1FF0h	Common RAM (Accesses 70h-7Fh)			
1C70h		1CF0h		1D70h		1DF0h		1E70h		1EF0h		1F70h		1FF0h				
1C7Fh		1CFFh		1D7Fh		1DFFh		1E7Fh		1EFFh		1F7Fh		1FFFh				

Note: 1. Available on 40/44-pin devices only

Legend:

■ Unimplemented data memory locations, read as '0'