Address	Device PIC18F27Q10 PIC18F47Q10

Note 1	Stack (31 Levels)

Address	Device PIC18F27Q10 / PIC18F47Q10
00 0000h	Reset Vector
…	…
00 0008h	Interrupt Vector High
…	…
00 0018h	Interrupt Vector Low
…	…
00 001Ah to 01 FFFFh	Program Flash Memory (64 KW)
02 0000h to 1F FFFFh	Not Present[2]
20 0000h to 20 00FFh	User IDs (128 Words)[3]
20 0100h to 2F FFFFh	Reserved
30 0000h to 30 000Bh	Configuration Words (6 Words)[3]
30 000Ch to 30 FFFFh	Reserved
31 0000h to 31 00FFh	Data EEPROM (1024 Bytes)
31 0100h to 31 01FFh	
30 000Ch to 30 FFFFh	Reserved
3F FFFCh to 3F FFFDh	Revision ID (1 Word)[4]
3F FFFEh to 3F FFFFh	Device ID (1 Word)[4]

Note 1: The stack is a separate SRAM panel, apart from all user memory panels.
   2: The addresses do not roll over. The region is read as '0'.
   3: Not code-protected.
   4: Device/Revision IDs are hard-coded in silicon.