# Nano Debugger

DEBUGGER SIDE

TARGET SIDE

| Interface / Signal | SWD TARGET | UPDI TARGET | ICSP™ TARGET |
|---|---|---|---|
| CDC TX | UART RX | UART RX | UART RX |
| CDC RX | UART TX | UART TX | UART TX |
| DBG0 | SWDIO | UPDI | DAT |
| DBG1 | SWCLK | N/A | CLK |
| DBG2 | N/A | N/A | N/A |
| DBG3 | RESET | RESET | MCLR |

## VBUS OVP AND START-UP DELAY

U101 NCP360SNAET1G

VBUS_DELAYED

VBUS OVERVOLTAGE PROTECTION:
Vin: 1.2V to 20V
Overvoltage Lockout Threshold: 6.25V

START-UP DELAY: 4ms

## VBUS CURRENT-LIMIT

U102 MIC2009A-1

CURRENT LIMIT:
- With R100 = 300ohm, the current through the power switch MIC2009A-1 is limited to: 507mA (min) - 687mA(typ) - 877mA (max).

## DEBUGGER REGULATOR

U103 MCP1755/3.3V

MCP1755:
Vin: 3.6V to 16V
Vout: Fixed 3.3V
Imax: 300mA
Dropout: 500mV @ 300mA

## TARGET VOLTAGE MEASUREMENT

VCC_TARGET (input) = 1.65V to 5.5V

VCC_TARGET needs to be supplied from target through CORTEX or UPDI pin header

VCC_TARGET range is limited by level shifter range

## RESET LEVEL SHIFTER (OPEN DRAIN)

Q100 DMN3002E-7-F

R106 is required to pull the Q100 gate to a defined value when the U100 is not powered

## DEBUGGER

ATSAMD21E18A U100

## DEBUGGER USB-C CONNECTOR

J100 USB4215-03-A

## LEVEL SHIFTERS (BIDIRECTIONAL)

U104 U105 U106 U107 74LVC1T45DW-7

## CORTEX 10-PIN HEADER

J101 HDR-1.27 Male 2x5 Shrouded

## SIL PIN HEADER

J102 HDR-2.54 Male 1x5

## UART PIN HEADER

J103 HDR-2.54 Male 1x4

## MOUNTING HOLES

TP102 TP103 TP104 TP105

## DEBUGGER POWER/STATUS LED

D100 GREEN

## CORTEX 10-PIN HEADER

J104 HDR-1.27 Male 2x5

Programming connector for factory programming of Debugger.

CSAMD Template Revision: 2.10

| | |
|---|---|
| Project Owner: | JB |
| PCB Layout Contact: | VL |
| PartNumber: | DV15P48A |
| Project Title | Nano Debugger |
| Variant: | Default Assembly |
| Sheet Title | Nano Debugger |
| Size | A3 |
| SCH #: | 02-01641 |
| PCB #: | 04-12671 |
| Rev: | 2 |
| Rev: | 1 |
| Date: | 08.05.2026 |
| Sheet | 1 of 2 |
| File: | Standalone_Nano_Debugger.SchDoc |

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