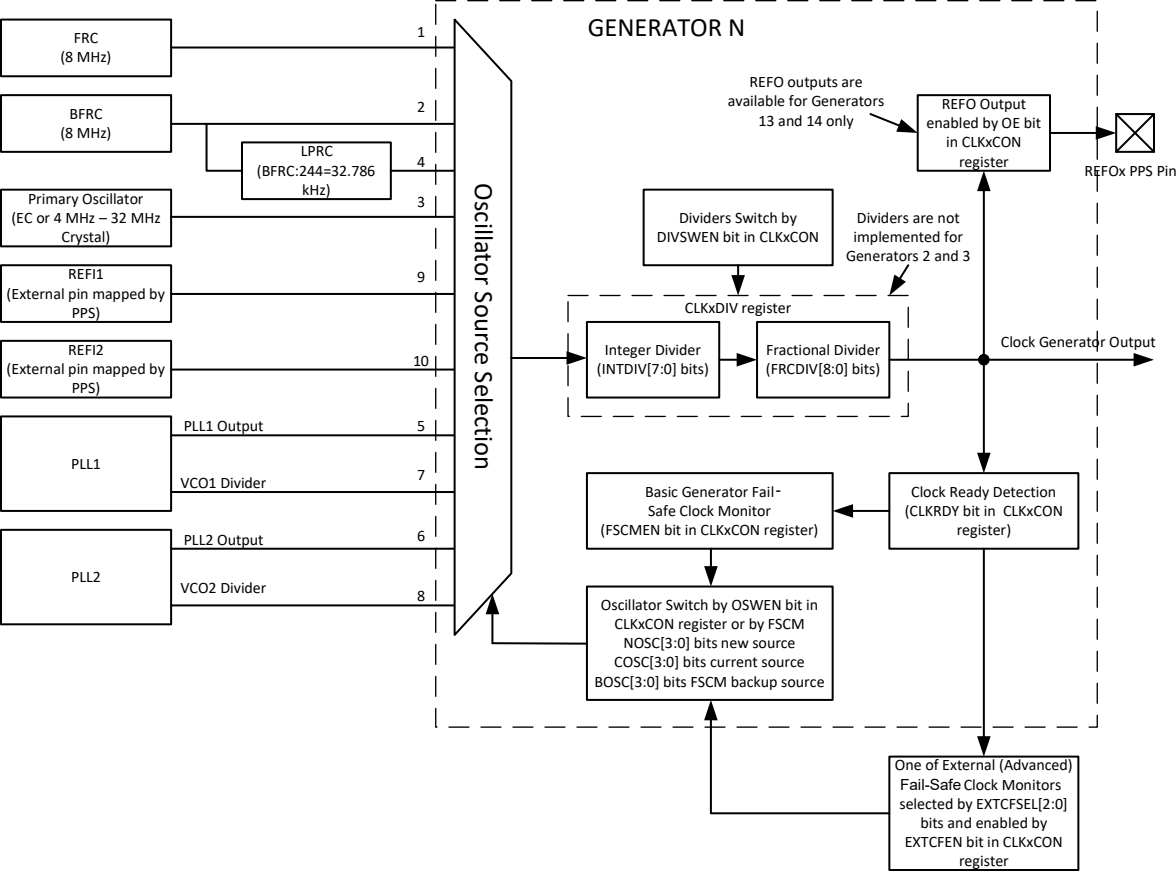
GENERATOR N
FRC
(8 MHz)
BFRC
(8 MHz)
LPRC
(BFRC:244=32.786
kHz)
Primary Oscillator
(EC or 4 MHz – 32 MHz
Crystal)
REFI1
(External pin mapped by
PPS)
REFI2
(External pin mapped by
PPS)
PLL1
PLL1 Output
VCO1 Divider
PLL2
PLL2 Output
VCO2 Divider
1
2
4
3
9
10
5
7
6
8
Oscillator Source Selection
REFO outputs are
available for Generators
13 and 14 only
REFO Output
enabled by OE bit
in CLKxCON
register
REFOx PPS Pin
Dividers Switch by
DIVSWEN bit in CLKxCON
Dividers are not
implemented for
Generators 2 and 3
CLKxDIV register
Integer Divider
(INTDIV[7:0] bits)
Fractional Divider
(FRCDIV[8:0] bits)
Clock Generator Output
Basic Generator Fail-
Safe Clock Monitor
(FSCMEN bit in CLKxCON register)
Clock Ready Detection
(CLKRDY bit in CLKxCON
register)
Oscillator Switch by OSWEN bit in
CLKxCON register or by FSCM
NOSC[3:0] bits new source
COSC[3:0] bits current source
BOSC[3:0] bits FSCM backup source
One of External (Advanced)
Fail-Safe Clock Monitors
selected by EXTCFSEL[2:0]
bits and enabled by
EXTCFEN bit in CLKxCON
register