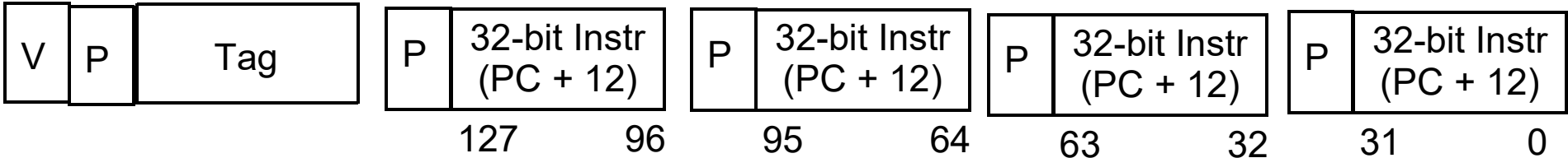
Tag address and valid bit

Instruction Cache Line (1 of N)