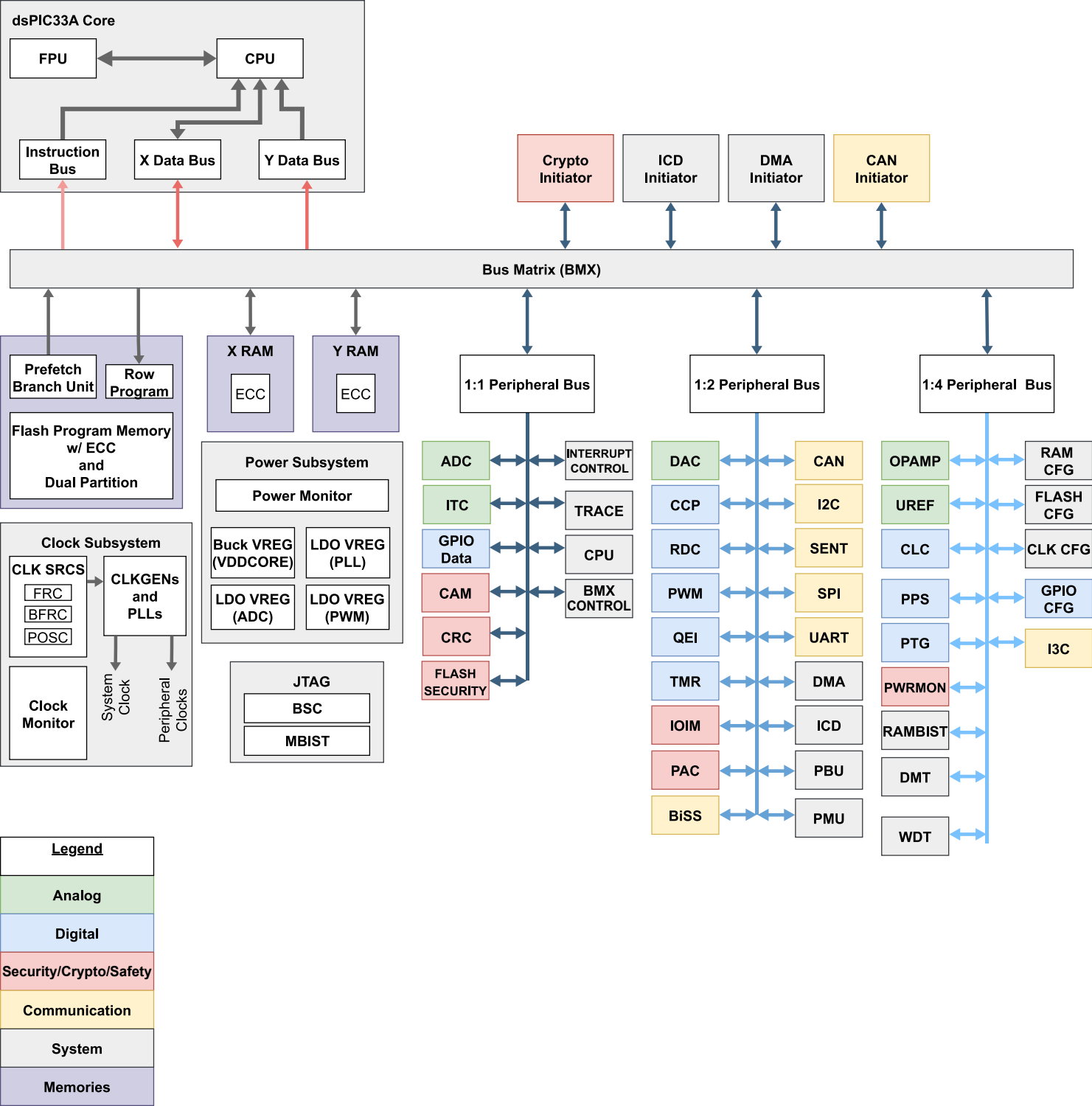
dsPIC33A Core
FPU
CPU
Instruction Bus
X Data Bus
Y Data Bus
Crypto Initiator
ICD Initiator
DMA Initiator
CAN Initiator
Bus Matrix (BMX)
Prefetch Branch Unit
Row Program
Flash Program Memory w/ ECC and Dual Partition
X RAM
ECC
Y RAM
ECC
Power Subsystem
Power Monitor
Buck VREG (VDDCORE)
LDO VREG (PLL)
LDO VREG (ADC)
LDO VREG (PWM)
Clock Subsystem
CLK SRCS
FRC
BFRC
POSC
CLKGENs and PLLs
Clock Monitor
System Clock
Peripheral Clocks
JTAG
BSC
MBIST
1:1 Peripheral Bus
ADC
ITC
GPIO Data
CAM
CRC
FLASH SECURITY
INTERRUPT CONTROL
TRACE
CPU
BMX CONTROL
1:2 Peripheral Bus
DAC
CCP
RDC
PWM
QEI
TMR
IOIM
PAC
BiSS
CAN
I2C
SENT
SPI
UART
DMA
ICD
PBU
PMU
1:4 Peripheral Bus
OPAMP
UREF
CLC
PPS
PTG
PWRMON
RAMBIST
DMT
WDT
RAM CFG
FLASH CFG
CLK CFG
GPIO CFG
I3C
Legend
Analog
Digital
Security/Crypto/Safety
Communication
System
Memories