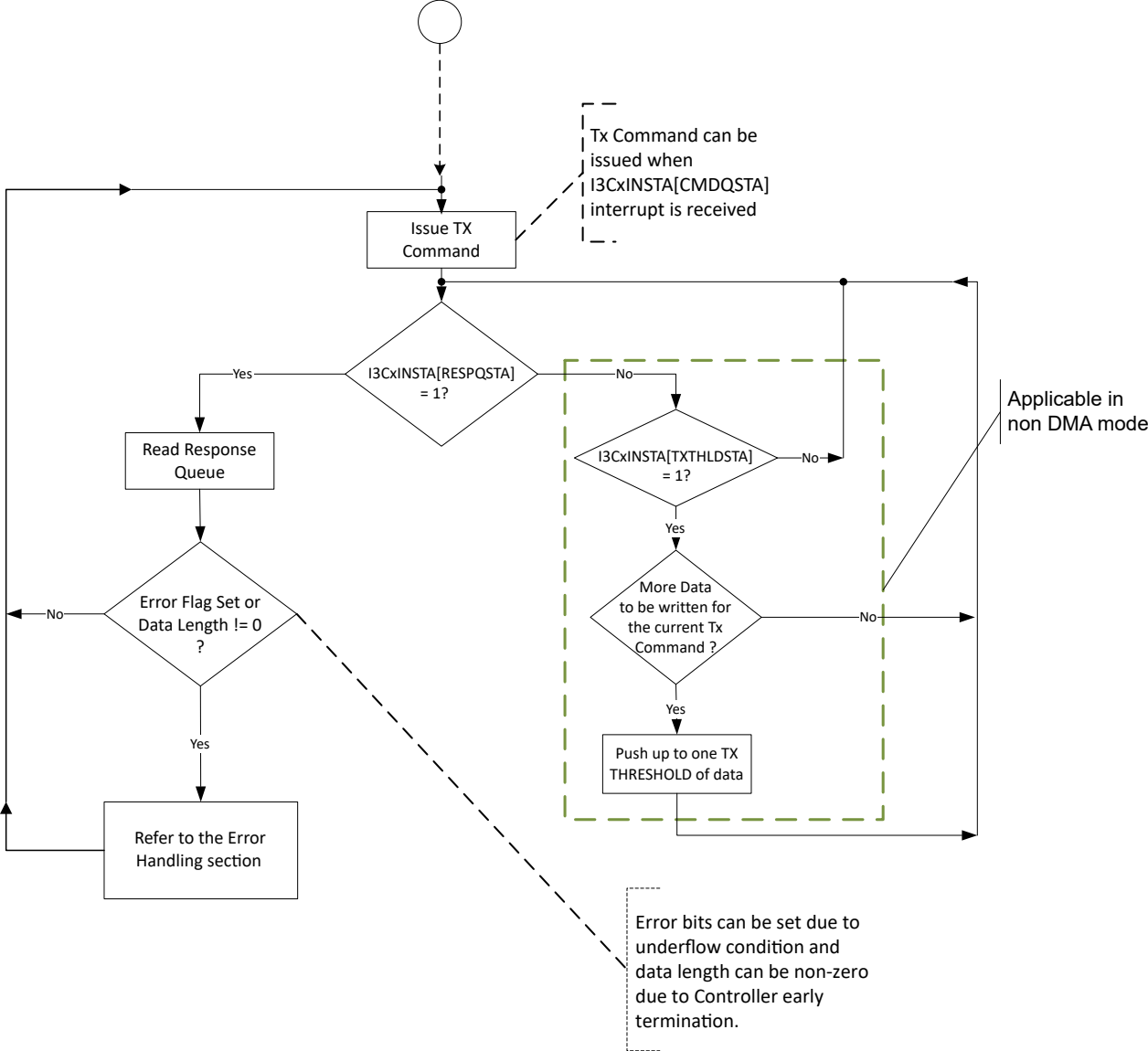
Tx Command can be issued when I3CxINSTA[CMDQSTA] interrupt is received
Issue TX Command
I3CxINSTA[RESPQSTA] = 1?
Yes
No
Read Response Queue
I3CxINSTA[TXTHLDSTA] = 1?
No
Yes
More Data to be written for the current Tx Command ?
No
Yes
Push up to one TX THRESHOLD of data
Applicable in non DMA mode
Error Flag Set or Data Length != 0 ?
No
Yes
Refer to the Error Handling section
Error bits can be set due to underflow condition and data length can be non-zero due to Controller early termination.