RDC Input Clock

ADC Sampling Trigger

RDCEXC

RDCEXCI

EXCSYNCEN Bit Status

Sync Start

$t_{sync}$

DONE Bit Status

PWM Output

(A) Settling time where excitation signal makes transition

(B) Sampling time where ADC is triggered by RDC and excitation signal is sampled by ADC

1 EXCSYNCEN is set

2 SYNCCNT is loaded into SYNCCNTSTAT

3 Synchronization begins

4 Synchronization ends and RDC starts generating excitation signals: RDCEXC and RDCEXCI

A Settling time where excitation signal makes transition

B Sampling time where ADC is triggered by RDC and excitation signal is sampled by ADC