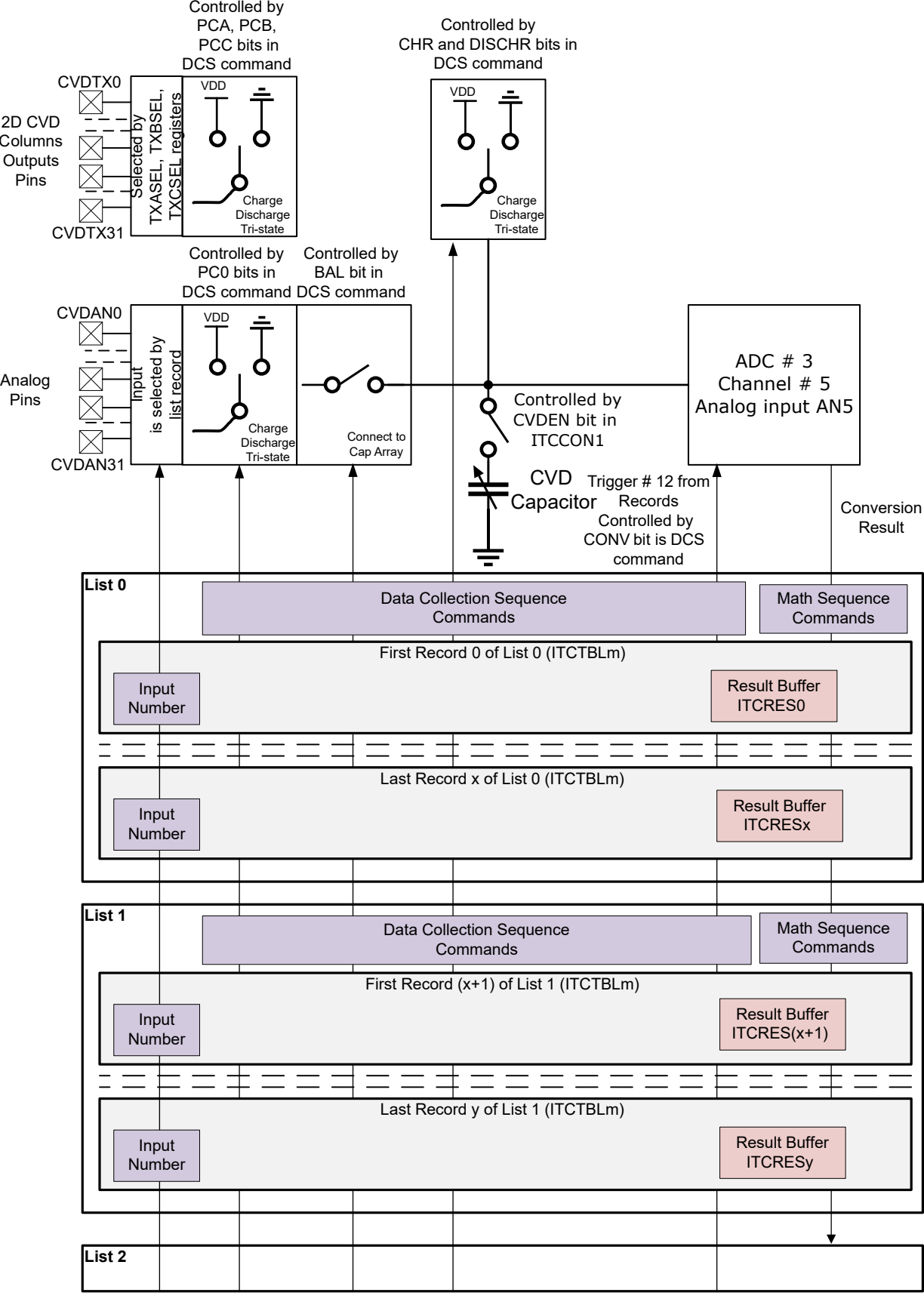
Controlled by PCA, PCB, PCC bits in DCS command
Controlled by CHR and DISCHR bits in DCS command
CVDTX0
2D CVD Columns Outputs Pins
CVDTX31
Selected by TXASEL, TXBSEL, TXCSEL registers
VDD
Charge
Discharge
Tri-state
Controlled by PC0 bits in DCS command
Controlled by BAL bit in DCS command
CVDAN0
Analog Pins
CVDAN31
Input is selected by list record
Connect to Cap Array
ADC # 3
Channel # 5
Analog input AN5
Controlled by CVDEN bit in ITCCON1
CVD Capacitor
Trigger # 12 from Records Controlled by CONV bit is DCS command
Conversion Result
List 0
Data Collection Sequence Commands
Math Sequence Commands
First Record 0 of List 0 (ITCTBLm)
Input Number
Result Buffer ITCRES0
Last Record x of List 0 (ITCTBLm)
Input Number
Result Buffer ITCRESx
List 1
Data Collection Sequence Commands
Math Sequence Commands
First Record (x+1) of List 1 (ITCTBLm)
Input Number
Result Buffer ITCRES(x+1)
Last Record y of List 1 (ITCTBLm)
Input Number
Result Buffer ITCRESy
List 2