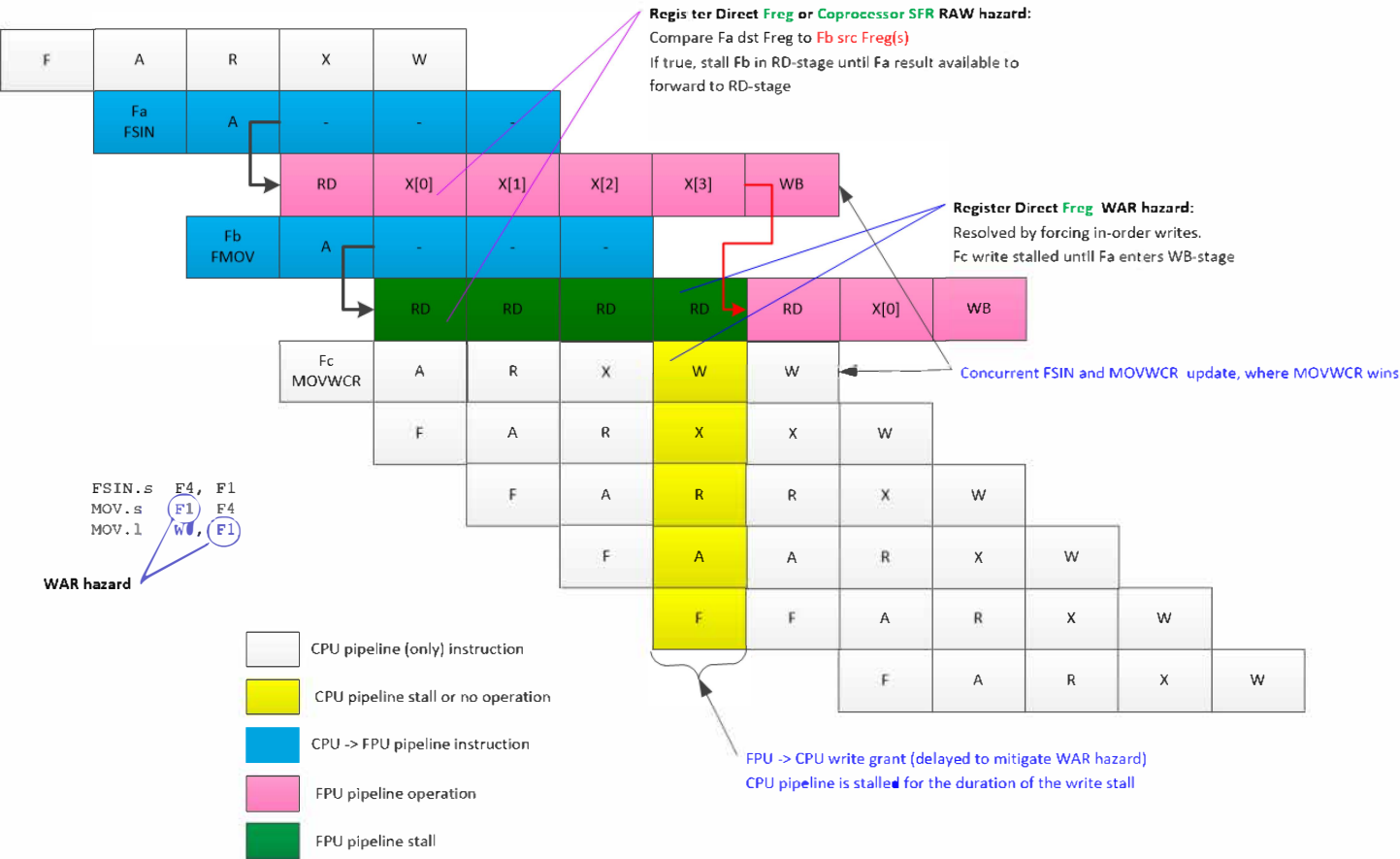
Regis ter Direct Freg or Coprocessor SFR RAW hazard:
Compare Fa dst Freg to Fb src Freg(s)
If true, stall Fb in RD-stage until Fa result available to forward to RD-stage
Register Direct Freg WAR hazard:
Resolved by forcing in-order writes.
Fc write stalled until Fa enters WB-stage
Concurrent FSIN and MOVWCR update, where MOVWCR wins
FSIN.s F4, F1
MOV.s F1 F4
MOV.l W0, F1
WAR hazard
F A R X W
Fa FSIN A - - -
RD X[0] X[1] X[2] X[3] WB
Fb FMOV A - - -
RD RD RD RD RD X[0] WB
Fc MOVWCR A R X W W
F A R X X W
F A R R X W
F A A R X W
F F A R X W
F A R X W
CPU pipeline (only) instruction
CPU pipeline stall or no operation
CPU -> FPU pipeline instruction
FPU pipeline operation
FPU pipeline stall
FPU -> CPU write grant (delayed to mitigate WAR hazard)
CPU pipeline is stalled for the duration of the write stall