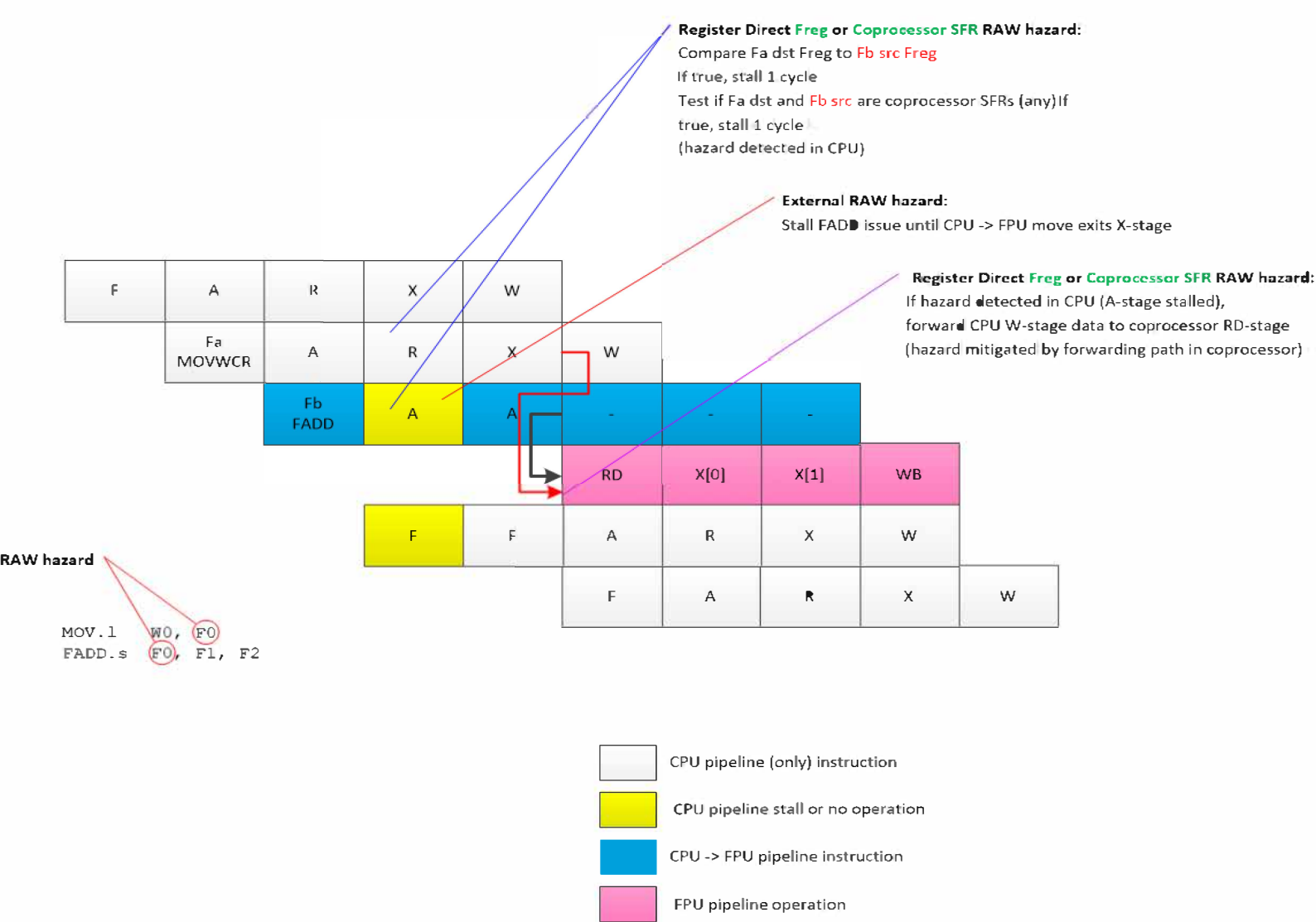
Register Direct Freg or Coprocessor SFR RAW hazard:
Compare Fa dst Freg to Fb src Freg
If true, stall 1 cycle
Test if Fa dst and Fb src are coprocessor SFRs (any)If true, stall 1 cycle
(hazard detected in CPU)
External RAW hazard:
Stall FADD issue until CPU -> FPU move exits X-stage
Register Direct Freg or Coprocessor SFR RAW hazard:
If hazard detected in CPU (A-stage stalled),
forward CPU W-stage data to coprocessor RD-stage
(hazard mitigated by forwarding path in coprocessor)
F
A
R
X
W
Fa
MOVWCR
Fb
FADD
-
RD
X[0]
X[1]
WB
RAW hazard
MOV.l W0, F0
FADD.s F0, F1, F2
CPU pipeline (only) instruction
CPU pipeline stall or no operation
CPU -> FPU pipeline instruction
FPU pipeline operation