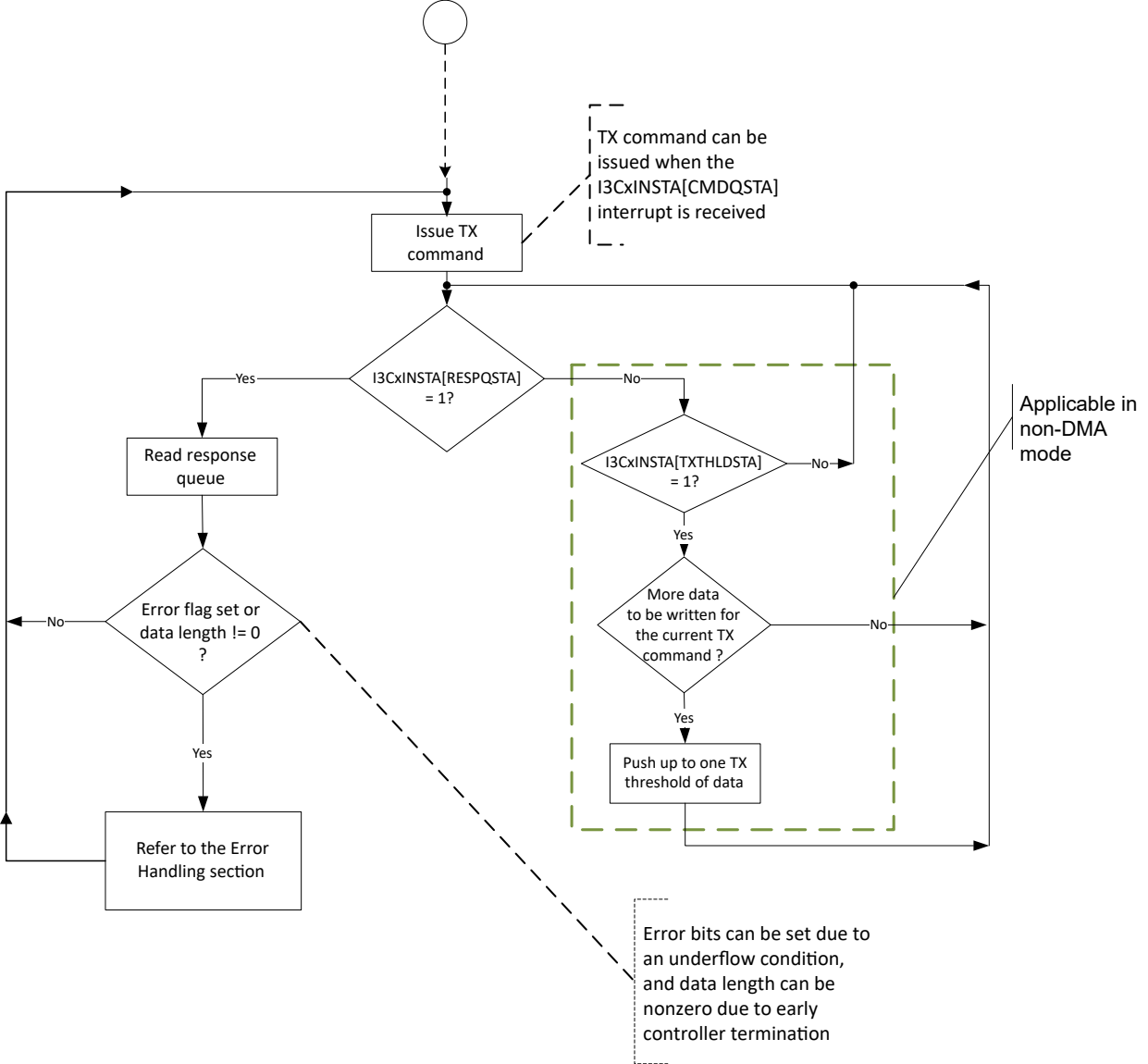
TX command can be issued when the I3CxINSTA[CMDQSTA] interrupt is received
Issue TX command
I3CxINSTA[RESPQSTA] = 1?
Yes
No
Read response queue
Error flag set or data length != 0 ?
No
Yes
Refer to the Error Handling section
I3CxINSTA[TXTHLDSTA] = 1?
No
Yes
More data to be written for the current TX command ?
No
Yes
Push up to one TX threshold of data
Applicable in non-DMA mode
Error bits can be set due to an underflow condition, and data length can be nonzero due to early controller termination