BANK 56

Address	Register
1C00h	Core Registers
1C0Bh	
1C0Ch–1C6Fh	Unimplemented Read as '0'
1C70h–1C7Fh	Common RAM (Accesses 70h-7Fh)

BANK 57

Address	Register
1C80h	Core Registers
1C8Bh	
1C8Ch	NVMADRL
1C8Dh	NVMADRH
1C8Eh	NVMDATL
1C8Fh	NVMDATH
1C90h	NVMCON1
1C91h	NVMCON2
1C92h	SCANCON0
1C93h	SCANLADRL
1C94h	SCANLADRH
1C95h	—
1C96h	SCANHADRL
1C97h	SCANHADRH
1C98h	—
1C99h	SCANDPS
1C9Ah	SCANTRIG
1C9Bh	—
1C9Ch	—
1C9Dh	CRCDATAL
1C9Eh	CRCDATAH
1C9Fh	CRCDATAU
1CA0h	CRCDATAT
1CA1h	CRCOUTL
1CA2h	CRCOUTH
1CA3h	CRCOUTU
1CA4h	CRCOUTT
1CA5h	CRCCON0
1CA6h	CRCCON1
1CA7h	CRCCON2
1CA8h	Unimplemented Read as '0'
1CEFh	
1CF0h–1CFFh	Common RAM (Accesses 70h-7Fh)

BANK 58

Address	Register
1D00h	Core Registers
1D0Bh	
1D0Ch	ADLTHL
1D0Dh	ADLTHH
1D0Eh	ADUTHL
1D0Fh	ADUTHH
1D10h	ADERRL
1D11h	ADERRH
1D12h	ADSTPTL
1D13h	ADSTPTH
1D14h	ADFLTRL
1D15h	ADFLTRH
1D16h	ADACCL
1D17h	ADACCH
1D18h	ADACCU
1D19h	ADCNT
1D1Ah	ADRPT
1D1Bh	ADPREVL
1D1Ch	ADPREVH
1D1Dh	ADRESL
1D1Eh	ADRESH
1D1Fh	ADPCH
1D20h	—
1D21h	ADACQL
1D22h	ADACQH
1D23h	ADCAP
1D24h	ADPREL
1D25h	ADPREH
1D26h	ADCON0
1D27h	ADCON1
1D28h	ADCON2
1D29h	ADCON3
1D2Ah	ADSTAT
1D2Bh	ADREF
1D2Ch	ADACT
1D2Dh	ADCLK
1D2Eh	ADCG1A
1D2Fh	ADCG1B
1D30h	ADCG1C
1D31h	ADCG1D[1]
1D32h	ADCG1E
1D33h	Unimplemented Read as '0'
1D6Fh	
1D70h–1D7Fh	Common RAM (Accesses 70h-7Fh)

BANK 59

Address	Register
1D80h	Core Registers
1D8Bh	
1D8Ch	RA0PPS
1D8Dh	RA1PPS
1D8Eh	RA2PPS
1D8Fh	RA3PPS
1D90h	RA4PPS
1D91h	RA5PPS
1D92h	RA6PPS
1D93h	RA7PPS
1D94h	RB0PPS
1D95h	RB1PPS
1D96h	RB2PPS
1D97h	RB3PPS
1D98h	RB4PPS
1D99h	RB5PPS
1D9Ah	RB6PPS
1D9Bh	RB7PPS
1D9Ch	RC0PPS
1D9Dh	RC1PPS
1D9Eh	RC2PPS
1D9Fh	RC3PPS
1DA0h	RC4PPS
1DA1h	RC5PPS
1DA2h	RC6PPS
1DA3h	RC7PPS
1DA4h	RD0PPS[1]
1DA5h	RD1PPS[1]
1DA6h	RD2PPS[1]
1DA7h	RD3PPS[1]
1DA8h	RD4PPS[1]
1DA9h	RD5PPS[1]
1DAAh	RD6PPS[1]
1DABh	RD7PPS[1]
1DACh	RE0PPS
1DADh	RE1PPS
1DAEh	RE2PPS
1DAFh	Unimplemented Read as '0'
1DCFh	
1DD0h	TRISC0PPS
1DD1h	TRISC1PPS
1DD2h	TRISC2PPS
1DD3h	TRISC3PPS
1DD4h	TRISC4PPS
1DD5h	TRISC5PPS
1DD6h	TRISC6PPS
1DD7h	TRISC7PPS
1DD8h	Unimplemented Read as '0'
1DEFh	
1DF0h–1DFFh	Common RAM (Accesses 70h-7Fh)

BANK 60

Address	Register
1E00h	Core Registers
1E0Bh	
1E0Ch	See Table 2 for register mapping details
1E6Fh	
1E70h–1E7Fh	Common RAM (Accesses 70h-7Fh)

BANK 61

Address	Register
1E80h	Core Registers
1E8Bh	
1E8Ch	See Table 3 for register mapping details
1EEFh	
1EF0h–1EFFh	Common RAM (Accesses 70h-7Fh)

BANK 62

Address	Register
1F00h	Core Registers
1F0Bh	
1F0Ch	UMTOAP
1F0Dh	UMTOAL
1F0Eh	UMTOAH
1F0Fh	Unimplemented Read as '0'
1F6Fh	
1F70h–1F7Fh	Common RAM (Accesses 70h-7Fh)

BANK 63

Address	Register
1F80h	Core Registers
1F8Bh	
1F8Ch	Unimplemented Read as '0'
1FE3h	
1FE4h	STATUS_SHAD
1FE5h	WREG_SHAD
1FE6h	BSR_SHAD
1FE7h	PCLATH_SHAD
1FE8h	FSR0L_SHAD
1FE9h	FSR0H_SHAD
1FEAh	FSR1L_SHAD
1FEBh	FSR1H_SHAD
1FECh	—
1FEDh	STKPTR
1FEEh	TOSL
1FEFh	TOSH
1FF0h–1FFFh	Common RAM (Accesses 70h-7Fh)

Note: 1. Available on 40/44-pin devices only

Legend:

Unimplemented data memory locations, read as '0'