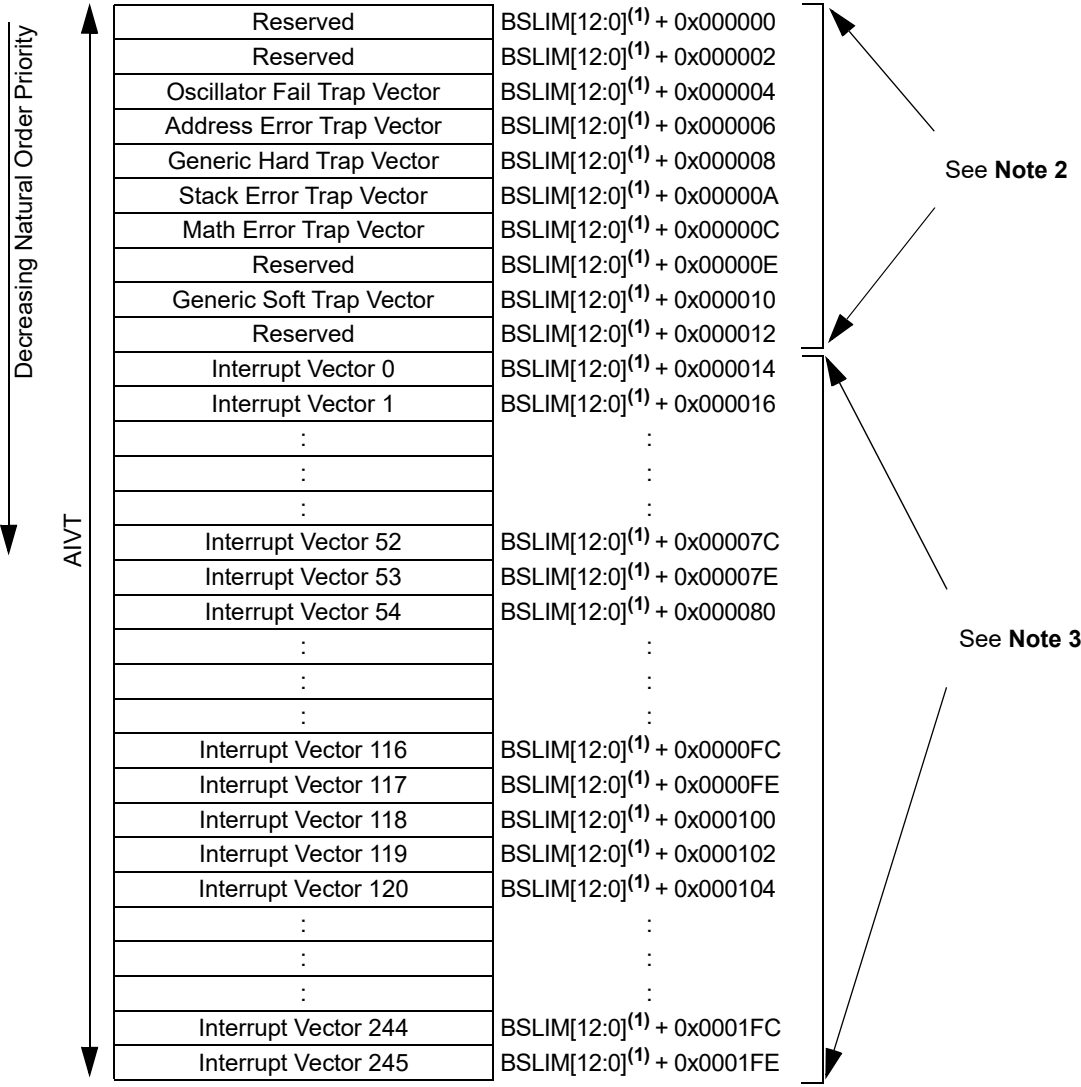
Decreasing Natural Order Priority
AIVT
Reserved
Reserved
Oscillator Fail Trap Vector
Address Error Trap Vector
Generic Hard Trap Vector
Stack Error Trap Vector
Math Error Trap Vector
Reserved
Generic Soft Trap Vector
Reserved
Interrupt Vector 0
Interrupt Vector 1
Interrupt Vector 52
Interrupt Vector 53
Interrupt Vector 54
Interrupt Vector 116
Interrupt Vector 117
Interrupt Vector 118
Interrupt Vector 119
Interrupt Vector 120
Interrupt Vector 244
Interrupt Vector 245
BSLIM[12:0](1) + 0x000000
BSLIM[12:0](1) + 0x000002
BSLIM[12:0](1) + 0x000004
BSLIM[12:0](1) + 0x000006
BSLIM[12:0](1) + 0x000008
BSLIM[12:0](1) + 0x00000A
BSLIM[12:0](1) + 0x00000C
BSLIM[12:0](1) + 0x00000E
BSLIM[12:0](1) + 0x000010
BSLIM[12:0](1) + 0x000012
BSLIM[12:0](1) + 0x000014
BSLIM[12:0](1) + 0x000016
BSLIM[12:0](1) + 0x00007C
BSLIM[12:0](1) + 0x00007E
BSLIM[12:0](1) + 0x000080
BSLIM[12:0](1) + 0x0000FC
BSLIM[12:0](1) + 0x0000FE
BSLIM[12:0](1) + 0x000100
BSLIM[12:0](1) + 0x000102
BSLIM[12:0](1) + 0x000104
BSLIM[12:0](1) + 0x0001FC
BSLIM[12:0](1) + 0x0001FE
See Note 2
See Note 3