BANK 62

1F00h 1F0Bh	Core registers
1F0Ch 1F0Fh	Unimplemented Read as '0'
1F10h	RA0PPS
1F11h	RA1PPS
1F12h	RA2PPS
1F13h	RA3PPS
1F14h	RA4PPS
1F15h	RA5PPS
1F16h 1F1Bh	Unimplemented Read as '0'
1F1Ch	RB4PPS(1)
1F1Dh	RB5PPS(1)
1F1Eh	RB6PPS(1)
1F1Fh	RB7PPS(1)
1F20h	RC0PPS(2)
1F21h	RC1PPS(2)
1F22h	RC2PPS(2)
1F23h	RC3PPS(2)
1F24h	RC4PPS(2)
1F25h	RC5PPS(2)
1F26h	RC6PPS(1)
1F27h	RC7PPS(1)
1F28h 1F37h	Unimplemented Read as '0'
1F38h	ANSELA
1F39h	WPUA
1F3Ah	ODCONA
1F3Bh	SLRCONA
1F3Ch	INLVLA
1F3Dh	IOCAP
1F3Eh	IOCAN
1F3Fh	IOCAF
1F40h 1F42h	Unimplemented Read as '0'
1F43h	ANSELB(1)
1F44h	WPUB(1)
1F45h	ODCONB(1)
1F46h	SLRCONB(1)
1F47h	INLVLB(1)
1F48h	IOCBP(1)
1F49h	IOCBN(1)
1F4Ah	IOCBF(1)
1F4Bh 1F4Dh	Unimplemented Read as '0'
1F4Eh	ANSELC(2)
1F4Fh	WPUC(2)
1F50h	ODCONC(2)
1F51h	SLRCONC(2)
1F52h	INLVLC(2)
1F53h	IOCCP(2)
1F54h	IOCCN(2)
1F55h	IOCCF(2)
1F56h 1F6Fh	Unimplemented Read as '0'
1F70h 1F7Fh	Common RAM (Accesses 70h-7Fh)

Note: 1. 20-pin devices only
2. 14/20-pin devices only

Legend:

Unimplemented data memory locations, read as '0'