BANK 56	BANK 57	BANK 58	BANK 59	BANK 60	BANK 61	BANK 62	BANK 63
1C00h	1C80h	1D00h	1D80h	1E00h	1E80h	1F00h	1F80h
Core Registers	Core Registers	Core Registers	Core Registers	Core Registers	Core Registers	Core Registers	Core Registers
1C0Bh	1C8Bh	1D0Bh	1D8Bh	1E0Bh	1E8Bh	1F0Bh	1F8Bh
1C0Ch	1C8Ch	1D0Ch	1D8Ch	1E0Ch	1E8Ch	1F0Ch	1F8Ch
				UMTOAP			
				1E0Dh			
				UMTOAL			
				1E0Eh			
				UMTOAH			
				1E0Fh			
Unimplemented Read as '0'	Unimplemented Read as '0'	Unimplemented Read as '0'	Unimplemented Read as '0'	Unimplemented Read as '0'	See Table 2 for register mapping details	See Table 3 for register mapping details	Unimplemented Read as '0'
							1FE3h
							1FE4h STATUS_SHAD
							1FE5h WREG_SHAD
							1FE6h BSR_SHAD
							1FE7h PCLATH_SHAD
							1FE8h FSR0L_SHAD
							1FE9h FSR0H_SHAD
							1FEAh FSR1L_SHAD
							1FEBh FSR1H_SHAD
							1FECh —
							1FEDh STKPTR
							1FEEh TOSL
1C6Fh	1CEFh	1D6Fh	1DEFh	1E6Fh	1EEFh	1F6Fh	1FEFh TOSH
1C70h Common RAM (Accesses 70h-7Fh)	1CF0h Common RAM (Accesses 70h-7Fh)	1D70h Common RAM (Accesses 70h-7Fh)	1DF0h Common RAM (Accesses 70h-7Fh)	1E70h Common RAM (Accesses 70h-7Fh)	1EF0h Common RAM (Accesses 70h-7Fh)	1F70h Common RAM (Accesses 70h-7Fh)	1FF0h Common RAM (Accesses 70h-7Fh)
1C7Fh	1CFFh	1D7Fh	1DFFh	1E7Fh	1EFFh	1F7Fh	1FFFh

Legend:

Unimplemented data memory locations, read as '0'