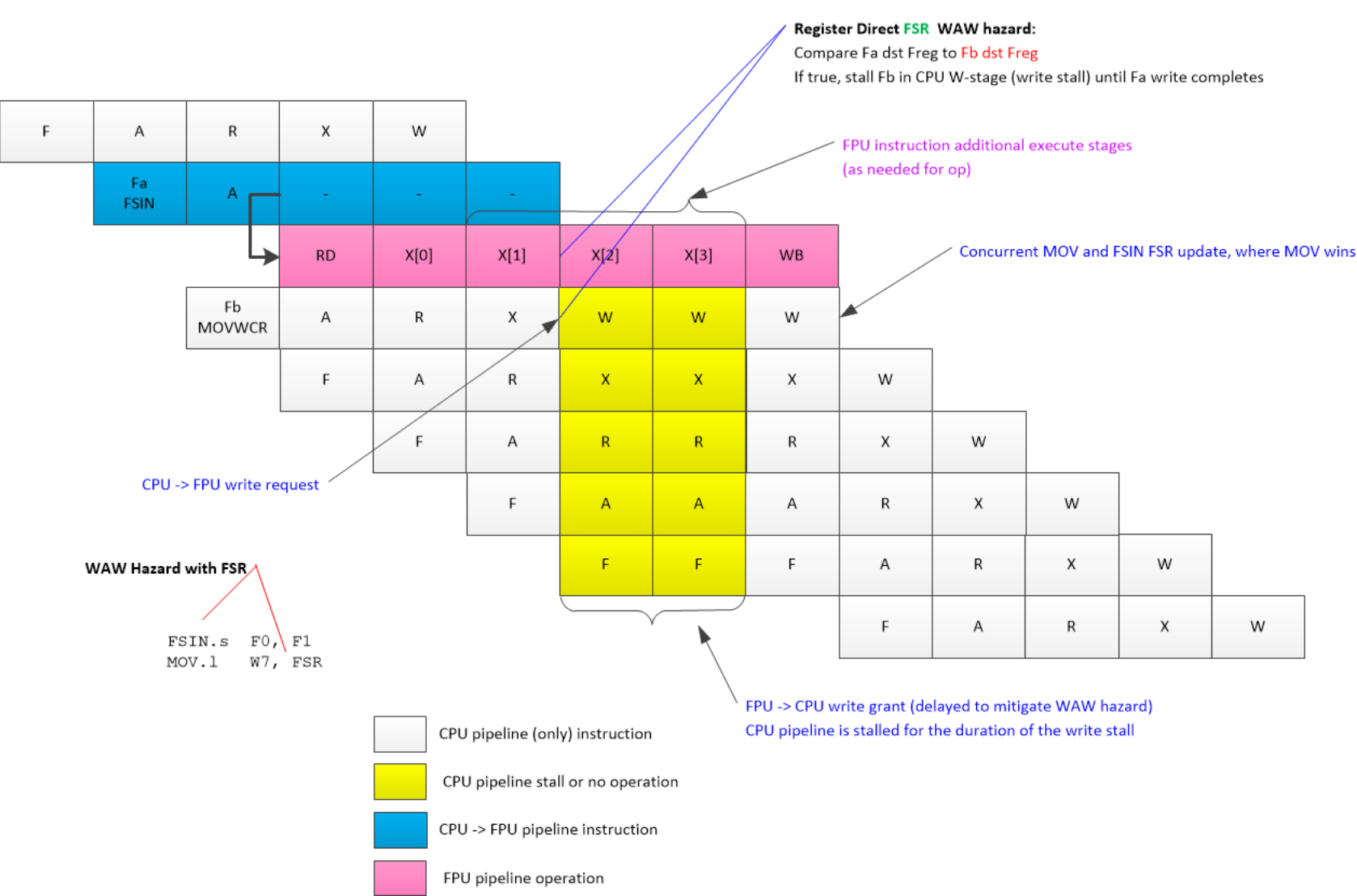
Register Direct FSR WAW hazard:
Compare Fa dst Freg to Fb dst Freg
If true, stall Fb in CPU W-stage (write stall) until Fa write completes
FPU instruction additional execute stages
(as needed for op)
Concurrent MOV and FSIN FSR update, where MOV wins
CPU -> FPU write request
WAW Hazard with FSR
FSIN.s F0, F1
MOV.l W7, FSR
FPU -> CPU write grant (delayed to mitigate WAW hazard)
CPU pipeline is stalled for the duration of the write stall
F A R X W
Fa FSIN A - - -
RD X[0] X[1] X[2] X[3] WB
Fb MOVWCR A R X W W W
F A R X X X W
F A R R R X W
F A A A R X W
F F F A R X W
F A R X W
CPU pipeline (only) instruction
CPU pipeline stall or no operation
CPU -> FPU pipeline instruction
FPU pipeline operation