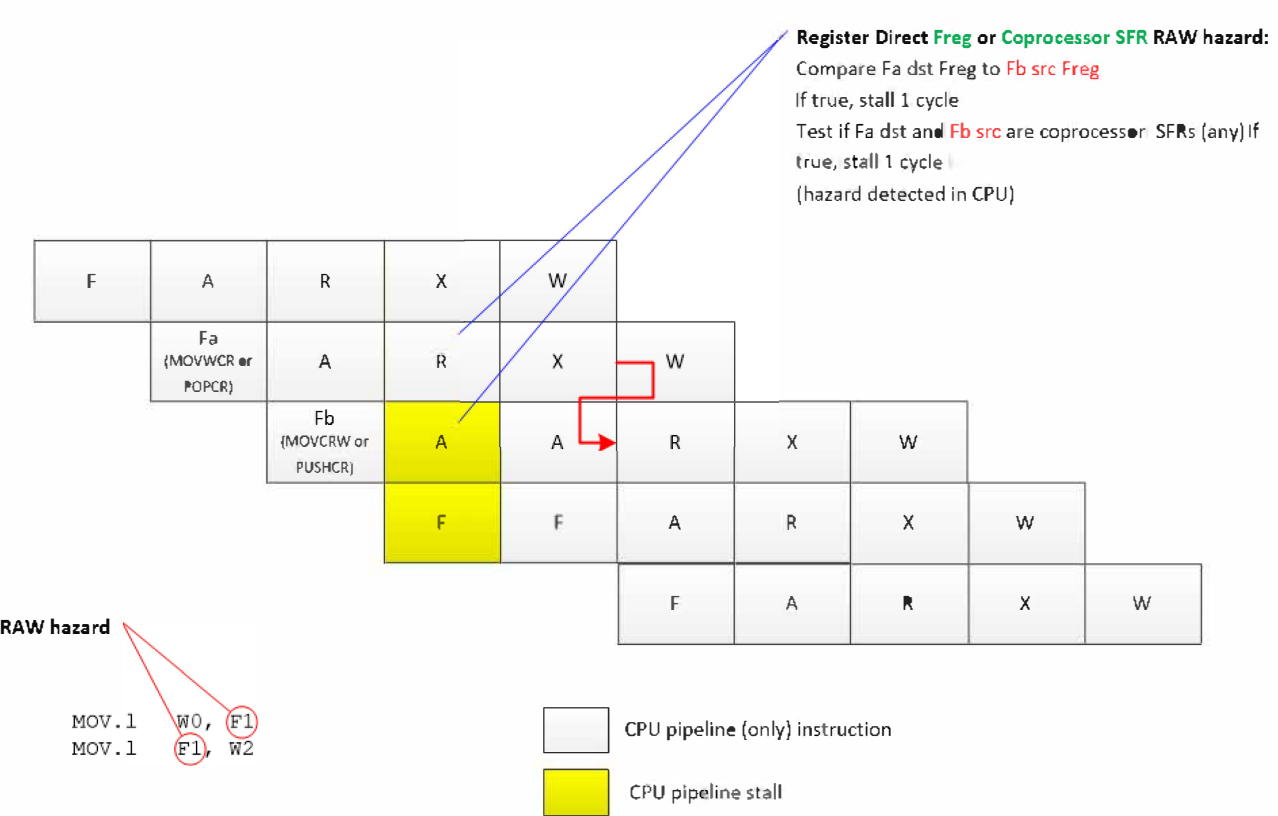
Register Direct Freg or Coprocessor SFR RAW hazard:
Compare Fa dst Freg to Fb src Freg
If true, stall 1 cycle
Test if Fa dst and Fb src are coprocessor SFRs (any) If true, stall 1 cycle
(hazard detected in CPU)
F
A
R
X
W
Fa (MOVWCR or POPCR)
Fb (MOVCRW or PUSHCR)
RAW hazard
MOV.l W0, F1
MOV.l F1, W2
CPU pipeline (only) instruction
CPU pipeline stall