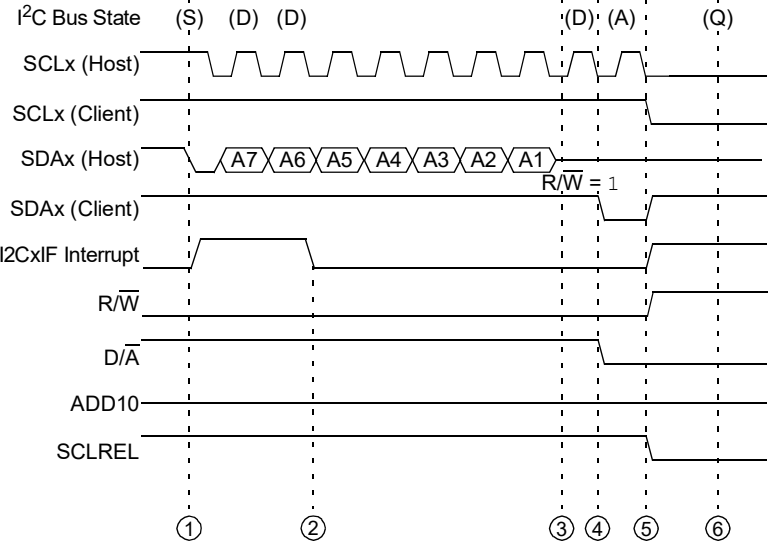

1. Detecting Start bit enables address detection. If SCIE is set, then interrupt will be asserted.
2. User software clears the interrupt flag.
3. R/$\overline{W}$ = 1 indicates that the client sends data bytes.
4. Valid address of first byte clears D/$\overline{A}$ status bit. Client generates $\overline{ACK}$.
5. R/$\overline{W}$ status bit is set. Client generates interrupt. SCLREL is cleared. Client pulls SCLx low while SCLREL = 0.
6. Bus waiting. Client prepares to send data.