



- ① Detecting Start bit enables address detection. If SCIE is : then interrupt will be asserted.
- ② User software clears the interrupt flag.
- ③ All '0's and $R/\overline{W} = 0$ indicates a general call.
- ④ Valid address clears D/\overline{A} status bit and sets GCSTAT status bit. Client generates \overline{ACK} . Address is loaded into I2CxRCV register.
- ⑤ R/\overline{W} status bit cleared. Client generates an interrupt.
- ⑥ Bus waiting. Client is ready to receive data.