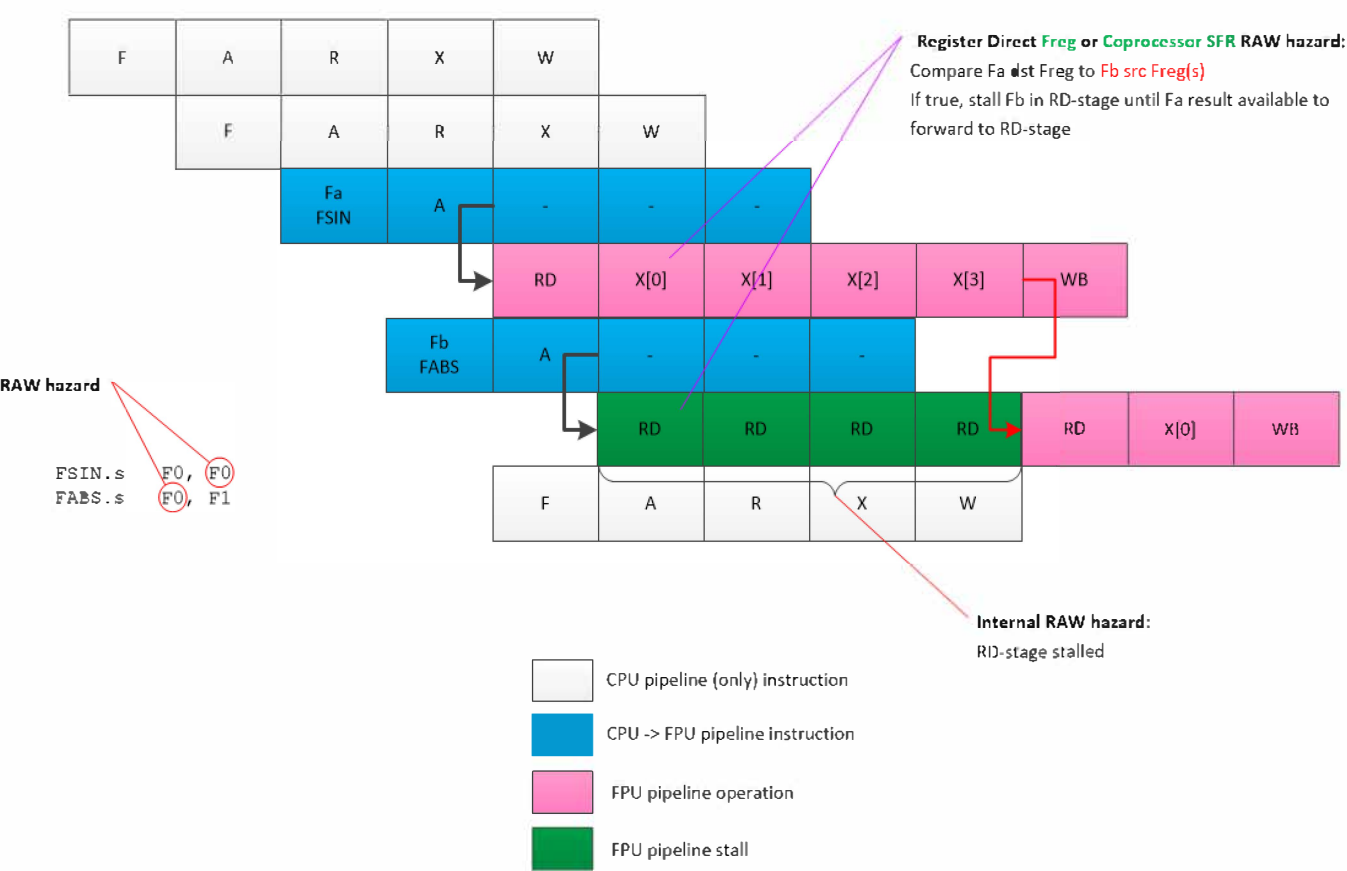
F
A
R
X
W
F
A
R
X
W
Fa
FSIN
A
-
-
-
RD
X[0]
X[1]
X[2]
X[3]
WB
Fb
FABS
A
-
-
-
RD
RD
RD
RD
RD
X[0]
WB
F
A
R
X
W
Register Direct Freg or Coprocessor SFR RAW hazard:
Compare Fa dst Freg to Fb src Freg(s)
If true, stall Fb in RD-stage until Fa result available to forward to RD-stage
RAW hazard
FSIN.s F0, F0
FABS.s F0, F1
Internal RAW hazard:
RD-stage stalled
CPU pipeline (only) instruction
CPU -> FPU pipeline instruction
FPU pipeline operation
FPU pipeline stall