Legend: F: Instruction Fetch / Pre-decode A: W-reg select / Read EA (RAGU) / Write EA (WAGU) R: Data Read / pre-MAC X: Execute 1 (ALU, multiply, divide iteration) W: Execute 2 (ACCx add/sub, shift, round) / Data Write Instruction read decode Instruction write decode X/Y RAGU and X WAGU Indirect address W-array write backs F Α R Χ W and MOVPAG target write /Integer SR read (as direct register) R Χ F Α Integer SR update (bit-wise) F Α R Χ W W F Α DSP SR update (bit-wise) Х W Α Result write-back to W-array, ACCx or EA F Α R Χ W Effective address calculated (Wb, Ws, Wd) F Α R Χ W Α R Χ W F F R Χ W Α