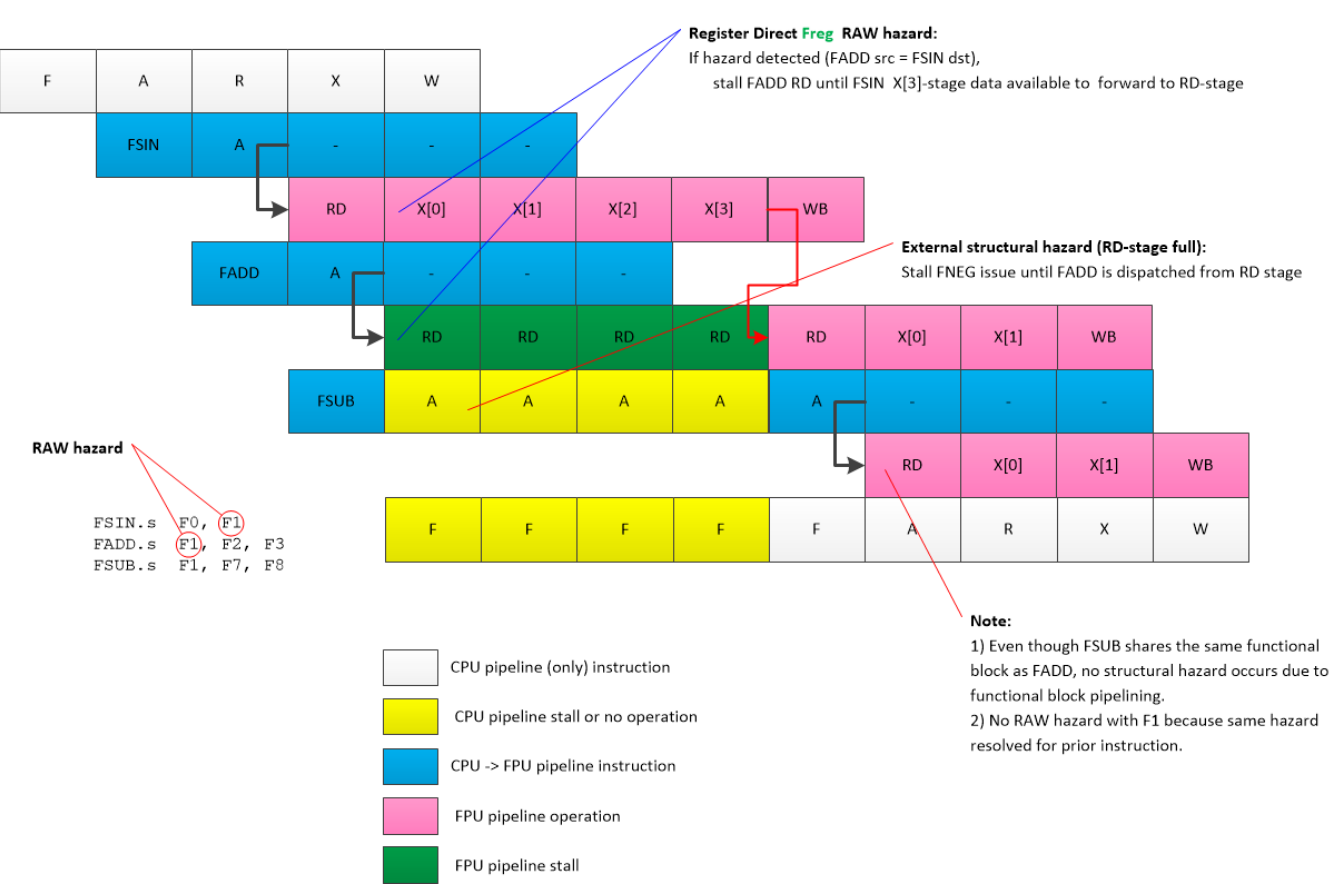
Register Direct Freg RAW hazard:
If hazard detected (FADD src = FSIN dst),
stall FADD RD until FSIN X[3]-stage data available to forward to RD-stage
External structural hazard (RD-stage full):
Stall FNEG issue until FADD is dispatched from RD stage
RAW hazard
FSIN.s F0, F1
FADD.s F1, F2, F3
FSUB.s F1, F7, F8
F A R X W
FSIN A - - -
RD X[0] X[1] X[2] X[3] WB
FADD A - - -
RD RD RD RD RD X[0] X[1] WB
FSUB A A A A A - - -
RD X[0] X[1] WB
F F F F F A R X W
Note:
1) Even though FSUB shares the same functional block as FADD, no structural hazard occurs due to functional block pipelining.
2) No RAW hazard with F1 because same hazard resolved for prior instruction.
CPU pipeline (only) instruction
CPU pipeline stall or no operation
CPU -> FPU pipeline instruction
FPU pipeline operation
FPU pipeline stall