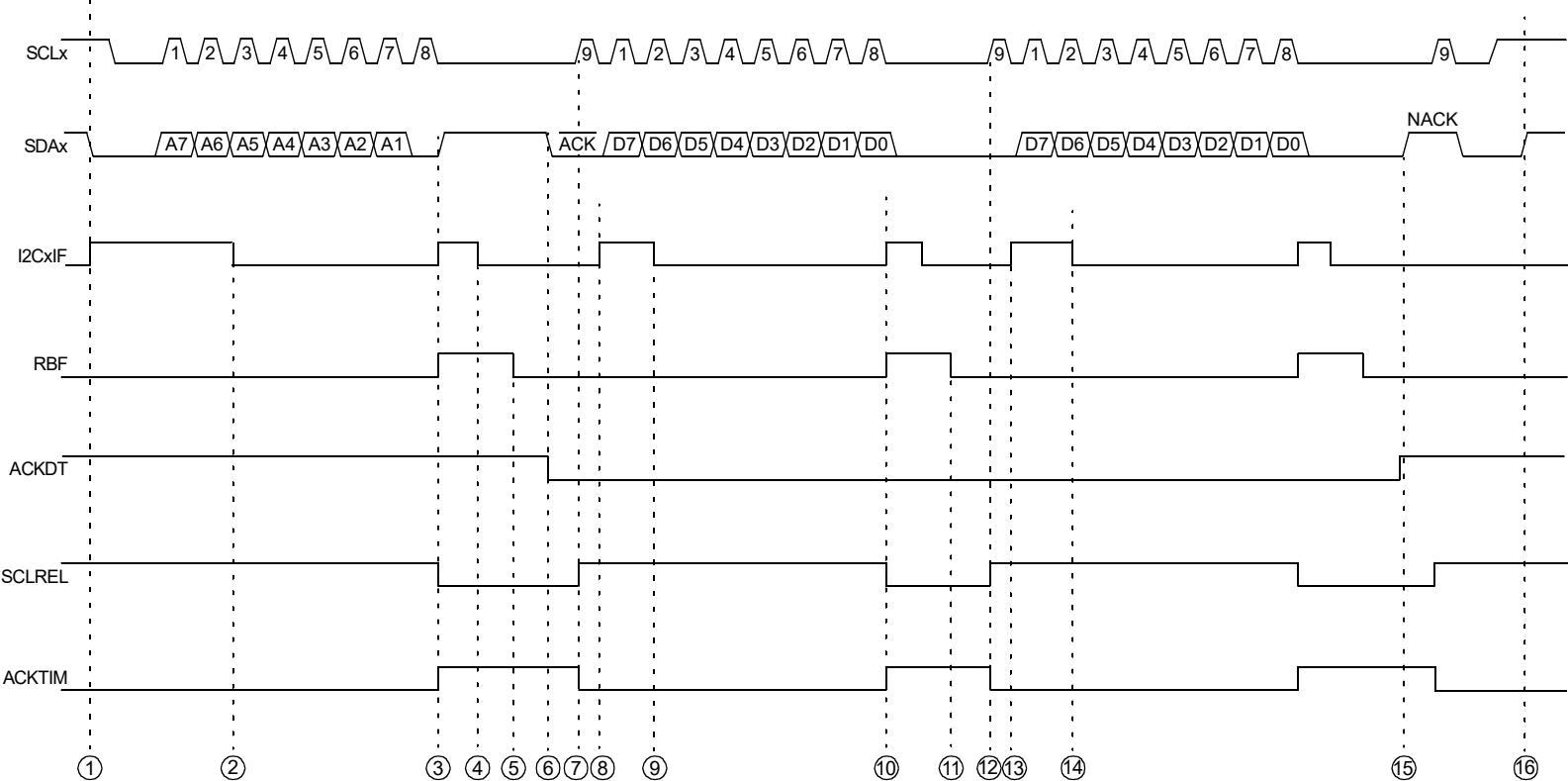




① Detecting Start bit enable address detection, interrupt flag is set if SCEN is set.

② User software clears the interrupt flag.

③ Client receives the address byte with $R/\overline{W} = 0$. Hardware clears SCLREL. Interrupt flag is asserted. ACKTIM is asserted. I2CxRCV is loaded with I2CxRSR and RBF is asserted.

④ User software clears the interrupt flag.

⑤ User software reads I2CxRCV, that clears the RBF flag.

⑥ ACKDT is written with $\overline{ACK}$ by user software.

⑦ User software sets SCLREL bit to release clock, ACKTIM is cleared by hardware.

⑧ Interrupt flag is set (not set if NACK is received).

⑨ User software clears the interrupt flag.

⑩ If DHEN = 1, hardware clears the SCLREL bit. I2CxRCV is loaded with I2CxRSR; ACKTIM is asserted at the end of eighth falling edge of SCLx by hardware.

⑪ User software reads I2CxRCV; clears the RBF flag.

⑫ User software releases the SCLREL bit, ACKTIM is cleared by hardware.

⑬ Interrupt flag is set.

⑭ User software clears the interrupt flag.

⑮ NACK.

⑯ Client recognizes the Stop event.