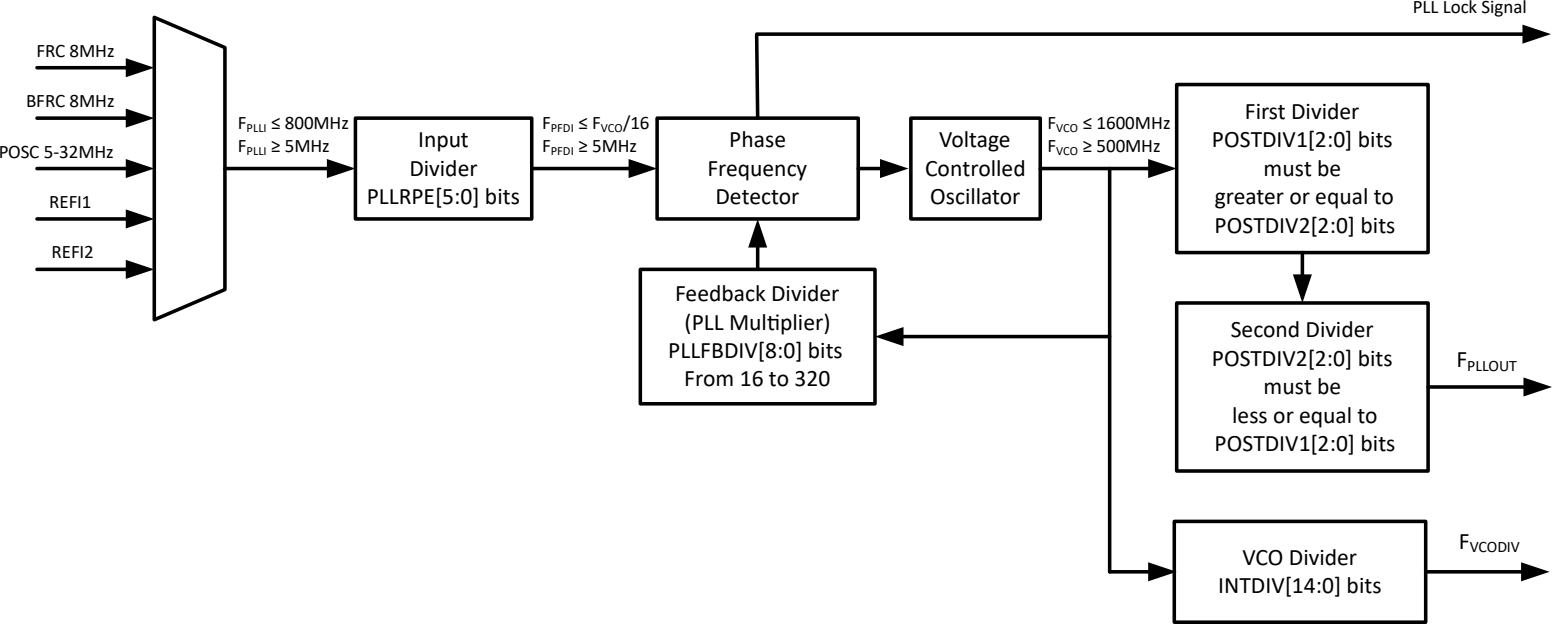
PLL Lock Signal
FRC 8MHz
BFRC 8MHz
POSC 5-32MHz
REFI1
REFI2
$F_{PLLI} \leq 800MHz$
$F_{PLLI} \geq 5MHz$
Input Divider PLLRPE[5:0] bits
$F_{PFDI} \leq F_{VCO}/16$
$F_{PFDI} \geq 5MHz$
Phase Frequency Detector
Voltage Controlled Oscillator
$F_{VCO} \leq 1600MHz$
$F_{VCO} \geq 500MHz$
First Divider POSTDIV1[2:0] bits must be greater or equal to POSTDIV2[2:0] bits
Feedback Divider (PLL Multiplier) PLLFBDIV[8:0] bits From 16 to 320
Second Divider POSTDIV2[2:0] bits must be less or equal to POSTDIV1[2:0] bits
F_{PLLOUT}
VCO Divider INTDIV[14:0] bits
F_{VCODIV}