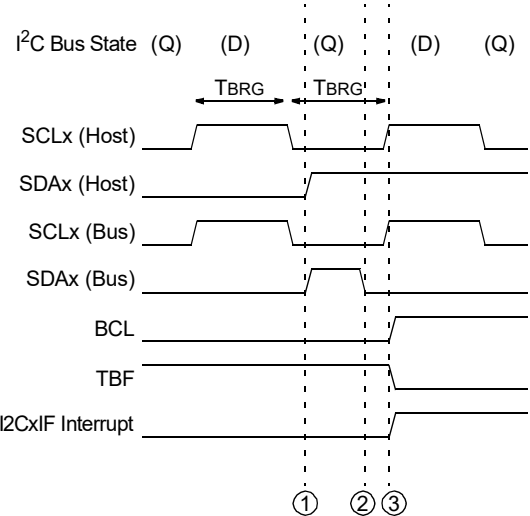

① Host transmits bit value of '1' in the next SCLx clock. Module releases SDAx.

② Another host on bus transmits the bit value of '0' in the next SCLx clock. Another host pulls SDAx low.

③ BRG times out. Module attempts to verify SDAx high. Bus collision detected.
Module releases SDAx and SCLx. Module sets BCL status bit and clears the TBF status bit. Host generates the interrupt.