Bit	7	6	5	4	3	2	1	0
	RUNSTDBY	SOURCE					MULFAC[1:0]	
Access	R/W	R/W					R/W	R/W
Reset	0	0					0	0
ľ	Bit 6 – SOUR	CE Select Sou	rce for PLI					
This bit controls the Phase-Locked Loop (PLL) clock source.								
	Value	Name		Description				
	0	OSCHF		High-frequency internal oscillator as PLL source				
	1 XOSCHF High-frequency external clock or external PLL source						gh-frequency o	oscillator as
_	D14 4 6 MILL		letali and an English					
Bits 1:0 – MULFAC[1:0] Multiplication Factor This bit field controls the multiplication factor for the Phased-Locked Loop (PLL).								
	Value	Name		Description				
	0x0 DISABLE PLL is disabled							
0x1 2x 2 x multiplication factor								
	0x2 3x 3x multiplication factor							
	0x3	- Reserved						