

Bit	7	6	5	4	3	2	1	0
	RUNSTDBY	SOURCE					MULFAC[1:0]	
Access	R/W	R/W					R/W	R/W
Reset	0	0					0	0

Bit 6 – SOURCE Select Source for PLL

This bit controls the Phase-Locked Loop (PLL) clock source.

Value	Name	Description
0	OSCHF	High-frequency internal oscillator as PLL source
1	XOSCHF	High-frequency external clock or external high-frequency oscillator as PLL source

Bits 1:0 – MULFAC[1:0] Multiplication Factor

This bit field controls the multiplication factor for the Phased-Locked Loop (PLL).

Value	Name	Description
0x0	DISABLE	PLL is disabled
0x1	2x	2 x multiplication factor
0x2	3x	3 x multiplication factor
0x3	-	Reserved